

Implementation of a Traffic Signal Controller using FPGA

林右文、陳慶順

E-mail: 9315039@mail.dyu.edu.tw

ABSTRACT

Field Programmable Gate Array and Complex Programmable Logic Device can control the circuit function and provide mass gates to implement complex circuit on single chip by user. The characteristics of FPGA are high capacity, low power consumption, high security and reprogrammable. This paper implements a 32-bits RISC processor by using Verilog HDL in association with the top-down design method from ASM behavioral description to hardware architecture. At last, simulation by SynapticCAD and implementation by FPGA are performed for rapid prototyping and verification of one traffic signal control logic.

Keywords : FPGA、HDL、RISC、ASM

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