以FPGA實現交通號誌控制器

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摘 要

現場可程式化邏輯閘陣列(Field Programmable Gate Array，FPGA)和複雜可程式邏輯元件(CPLD)可由使用者來控制電路功能並提供大量邏輯閘實現複雜電路於單一晶片中，具有高容量、低耗電量、高保密性及可重複燒錄的特性。本論文利用Verilog硬體描述語言(Hardware Description Language，HDL)實做一個32位元精簡指令集電腦(Reduced Instruction Set Computer，RISC)處理器，並運用由上而下的設計方法，以演算法狀態機(Algorithmic State Machine，ASM)將處理器從一個行為的動作描述實現成硬體架構。最後，配合SynaptiCAD模擬與Xilinx FPGA晶片快速成型驗證於交通號誌控制邏輯。

關鍵詞 : FPGA、HDL、RISC、ASM

目錄

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