

The Device Manufacture and ESD Characteristics Measurement in an Advanced IGBT

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ABSTRACT

In this thesis, an advanced IGBT device was simulated by using of three dimension simulation tool-Davinci, which could simulate the three dimension device structure and analyze the device characteristics. Meanwhile, the Davinci also could be used to design the physical parameters in manufacturing process, and it will exactly accomplish the object of device designing. The advanced IGBT is mainly toward improve the power performance. However, the device should be operated at high current density and high voltage situation. Thus, to reduce the loss of power performance, the device need to be haven the lower on-resistance and the fast switching speed in the forward conduction. Finally, in order to avoid the ESD(Electrostatic Discharge) damage, which could be caused the breakdown of gate oxidation, the IGBT device will be added the zener diode for the ESD protection consideration. Key words : Power performance, On-resistance, Switching speed, ESD, Zener diode

Keywords : Power performance ; On-resistance ; Switching speed ; ESD ; Zener diode

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REFERENCES

- 1] C.A.T. Salama, " V-groove Power MOSFET " ,IEDM,pp.409-412 1977.
- [2] D. Ueda et al. " A new injection suppression structure for conductivity modulated power MOSFET, " in Proc.18th Int. Conf.Solid State Device and Materials,vol.31. p.97,1986.
- [3] A.A.Tamer,K.Rauch,and J.L.Moll, " Numerical comparison of DMOS,VMOS,and UMOS power transistors " ,IEEE Trans. Electron Devices,vol. ED-30,p.73,1983.
- [4] M. Nandakumar, M. S. Shekar,and B. J. Baliga, " Fast switching power MOS-gated (EST and BRT) thyristors, " in IEEE Int. Symp. on Power Semiconductor Devices and ICs,1992,pp.255-258.
- [5] S.Kunori,J.Ishida,M.Tanaka,M.Watanabe,and T.Kan, " The low power dissipation Schottky barrier diode with trench structure, " in IEEE Int. Symp. Power Semiconductor Devices and ICs,1992,pp.66-71.
- [6] S.M.Sze, " Modern Semiconductor Device Physics " , A Wiley Interscience publication,1998,pp.225-226.

- [7] F. Udrea, and G. A. J. Amaratunga, " The New Generation of Power Semiconductor Devices " ,IEEE,1996,pp.468-476.
- [8] Yoshifumi Tomomatsu, John F. Donlon, Eric R. Motto, Hideo Iwamoto, Hideki Haruguchi, " A new punch through IGBT having a new N-buffer layer " , Proc. of the IEEE, pp.690-700, 1999.
- [9] Y. Onishi, S. Momota, Y. Kondo, M. Otsuki, N. Kumagai and K. Sakurai, " Analysis on Device Structures for Next Generation IGBT " ,pp.85-88,1998.
- [10] M. Sweet, S. Hardikar, O. Spulber, E. M. Sankara Narayanan, M. M. De Souza, Subhas Chandra Bose J.V., " The Trench Planar Insulated Gate Bipolar Transistor (TPIGBT), pp.13/1-13/5, 1999.
- [11] B. J. Baliga, M. S. Adler, P. V. Gray, and R. P. Love, " Suppressing latch-up in insulated gate transistors, " IEEE Electron Dev. Lett. pp.323,1984.
- [12] B. J. Baliga, " Power Semiconductor Device " .Boston, M.A:PWS, Ch8 pp.476-482,1995.
- [13] Sze, S. M. Semiconductor Devices: Physics and Technology. New York: Wiley, 1985.
- [14] Sze, S. M. Physics of Semiconductor Devices. 2nd ed. New York: Wiley, 1981.
- [15] Werner, W. M. " The Work Function Difference of the MOS System with Aluminum Field Plates and Polycrystalline Silicon Field Plates. " Solid State Electronics pp.769-75,1974.
- [16] Charvaka Duvvury, Fred Carvajal, Clif Jones, and David Briggs, " Lateral DMOS Design for ESD Robustness, " IEDM pp.375-378,1997.
- [17] Ajith Amerasekera, Charvaka Duvvury, " ESD in Silicon Integrated Circuits, " John Wiley & Sons, 1996.
- [18] R. zezulka, " ESD basics " EOS/ESD Tutorial Notes, 1993.
- [19] ANSI/EOS/ESD-DS5.2, EOS/ESD Association, Inc, 1996.
- [20] MIL-STD-883E, Method 3015.7, 1989.