The Investigation of Low Voltage High Speed CMOS Circuit on SOI Substrate

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ABSTRACT

The thesis describes the SOI is applied to the inverter which input a small dynamic signal to get its power consumption, and speed. To compare the value of the small dynamic with the bulk MOS, the variability of channel length can be the main factor in order to get the best low power and high speed performance in the experiment. The shorter channel length is, the speed is faster. However, the power consumption will get more speed by carrier run in the channel length. So the thesis investigates to find the best value of the high speed and low power performance device under the power-speed product. According to the result, the best power- speed product performance with the channel length is 0.25um.

Keywords : 絕緣體上矽 ; 功率速度乘積 ; 高速度 ; 低功率消耗

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