高速度、低電壓電路上使用絕緣層上磊晶矽製程之特性研究

蔡政村、王木俊 ; 王立民

E-mail: 9314893@mail.dyu.edu.tw

摘 要

本論文描述出一個SOI（Silicon on Insulator，絕緣體上矽）應用在一個反相器當中（Inverter）並輸入一動態小訊號，求其動態消耗功率，以及其速度，並與傳統(Bulk)的MOS元件做比較，以通道長度作為變化的主要原因去探討，求得最好的低功率消耗以及高速度元件。在通道長度縮短情況之下，速度會加快，但是功率消耗卻因為載子的熱量消耗，卻因此而上升，故本文探討找尋在功率速度乘積(Power-Speed Product)下找尋一個最好的值，以求得高速低功率元件， 經由數據的探討得知，在通道長度0.25um情況之下，可以得到最好的功率速度乘積(Power-Speed Product)。

關鍵詞 : 絕緣體上矽 ; 功率速度乘積 ; 高速度 ; 低功率消耗

目錄

參考文獻

[1] Fenouillet-Beranger, C.;et al. ,,“ Characterization and simulation of STI isolation for 0.1 μm partially-depleted SOI devices, SOI Conference, 2001 IEEE International , 1-4 Oct. 2001 Pages:87 - 88 J.J.Welser, ”Nanoscale CMOS”, Proc.IEEE,vol.87,pp.537-570.Apr.1990. [2] A.O.Adan, T.Naka, A. Kagisawa, and H.Shimizu,“ SOI As a Mainstream IC Technology, ” SOI Conference, 1998. Proceedings., 1998 IEEE International , 5-8 Oct. 1998 Pages:9 - 12 [3]James B.Kuo ; Ler-Wei Su ” CMOS VLSI Engineerin Silicon-on-Insulator (SOI)“ KLUWER ACADEMIC published , Boston. 1998.

[4] Mercha, A.; Rafi, J.M.; Simoen, E.; Augendre, E.; Claeys, C.; "Linear kink effect induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETS Electron Devices”, IEEE Transactions on , Volume: 50 , Issue: 7 , July 2003 Pages:1675 - 1682 [5] Delatte, P.; Brodeoux, V.; Lorent, P.; Flandre, D ” Comparison of 0.25 μm bulk, PD and FD SOI CMOS implementations of a low-voltage low-power programmable DLL for linear delay generation ” SOI Conference, 2000 IEEE International , 2-5 Oct. 2000 Pages:92 - 93 [6] Marshall, A.; Natarajan, S.;“ PD-SOI and FD-SOI: a comparison of circuit performance ” Electronics, Circuits and Systems, 2002. 9th International Conference on , Volume: 1 , 15-18 Sept. 2002 Pages:25 - 28 vol.1 [7]J. P. Colinge,“ Performances of low-voltage, low-power SOI CMOS

Technology ” Microelectronics, 1997. Proceedings., 1997 21st International Conference on , Volume: 1 , 14-17 Sept. 1997 Pages:229 - 236 vol.1 [8]Sun-Mo Kang Yusuf Leblebici; “ CMOS Digital Integrated Circuits Analysis and Design ” McGRAW HILL publish.2003 [9]Kaushik Roy, Sharcat C. Prasad “ Low-Power CMOS VLSI Circuit Design :Chapter 2.3.1 Short-Circuit Dissapation ” John Wiley Publishing, 2000 [10]Douglas A Pucknell Kamran Esragnian “ Basic VLSI Design ” Prentice Hall published, 1994 [11] Ying-Che Tseng; Huang, W.M.; Monk, D.J.; Welch, P.; Ford, J.M.; Woo, J.C.S.; ” AC floating body effects and the resultant analog circuit issues in submicron floating body and body-grounded SOI MOSFET's ” IEEE Electron Devices, 1999 Pages:1685 — 1692 [12] Pelloie, J.L.; Auberton-Herv, A.J.; Raynaud, C.; Faynot, O.; SOI technology performance and modeling IEEE Solid-State Circuits Conference 15-17 Feb. 1999 [13] Mercha, A.; Rafi, J.M.; Simoen, E.; Augendre, E.; Claeys, C ” "Linear kink effect induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETS ” IEEE Electron Devices, July 2003 Pages:1675 - 1682 [14] Berger, R.; Lyons, W.G.; Soares, A.; ” A 1.3 GHz SOI CMOS test chip for low-power high-speed pulse processing ” Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 8 , Aug. 1998 [15] Marshall, A.; Natarajan, S.; PD-SOI and FD-SOI: a comparison of circuit performance Electronics, Circuits and Systems, 2002. 9th International Conference on , Volume: 1 , 15-18 Sept. 2002 Pages:25 - 28 vol.1 [16] Fiegna, C.; Abramo, A.; Simulation of tunneling gate current in ultra-thin SOI MOSFETs; Semiconductor Device Research Symposium, 2001 International , 5-7 Dec. 2001 Pages:110 — 113 [17] Knoch, J.; Lengeler, B.; Appenzeller, J.; Quantum simulations of an ultrashort channel single-gated n-MOSFET on SOI; Electron Devices, IEEE Transactions on , Volume: 49 , Issue: 7 , July 2002 Pages:1212 - 1218