Variable Ordering Optimization for OBDD

張世龍、林浩仁

E-mail: 9314763@mail.dyu.edu.tw

ABSTRACT

OBDD (Ordered binary decision diagrams) is the most popular data structure for Boolean function representation in modern logic synthesis/verification EDA tools. It is obvious that the variable ordering is the key factor for reducing the size (nodes) of an OBDD. Therefore, how to find an effective variable order is the most critical issue during OBDD construction. Observing the constructed OBDD of a given variable order, we find that the number of nodes of the OBDD is proportional to the number of branches of the OBDD. Based on this observation, we propose an algorithm for deciding the variable order based on the 0/1 difference between the variables. Experimental results on LGSYNTH 93 benchmark circuits show that our approach is very effective for determining the variable order to reduce the size of OBDD.

Keywords : variable ordering ; ROBDD ; logic synthesis ; VLSI/CAD

Table of Contents

REFERENCES

[1] Bollig, B.; Wegener, I., “Improving the variable ordering of OBDD’s is NP-complete,” IEEE Transactions, Vol. 45, Pages: 993-1002, Sep 1996.

[2] B. Bolling, M. Lobbing, and I. Wegener, “On the effect of local changes in the variable ordering of ordered decision diagrams,” Inform. Processing Lett., vol. 59, Pages: 233-239, Oct 1996.

[3] C. Scholl, D. Moller, and P. Molitor, “BDD minimization Using Symmetries,” IEEE Trans. Computer-Aided Designs of Integrated Circuits and Systems, vol. 18, Feb 1999.

[4] D. Moller and R. Drechsler, “Symmetry based variable ordering for ROBDD’s,” in Proc. IFIP Workshop on Logic and Architecture Synthesis, Pages: 47-53, Dec 1994.

[5] William Hung, Adnan Aziz, and Ken McMillan, ”Heuristic Symmetry Reduction for Invariant Verification,” International Workshop on Logic Synthesis, Tahoe City, CA.1997.

[6] Hung, W.N.N.; Xiaoyu Song; Aboulhamid, E.M.; Driscoll, M.A., ” BDD minimization by scatter search, ” Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions, Vol. 21, Pages:974-979, Aug 2002.
[7] N. Zhuang, M.S.T. Benten, P.Y.K. Cheung, "Improved Variable Ordering of BDDS with Novel Genetic Algorithm," IEEE International Symposiums on Circuits and Systems, Atlanta May 1996.
[8] N. Ishiura, H. Sawada, and S. Yajima, “ Minimization of binary decision diagrams based on exchange of variables, ” in Proc. Int. Conf. Computer-Aided Design, Pages: 472-475, Nov 1991.
[9] R.E. Bryant, “ Graph-Based Algorithm for Boolean Function Manipulation, ” IEEE Trans. Computers, vol. 35, no. 8, Pages: 677-691, 1986.
[10] Rudell, R., ” Dynamic variable ordering for ordered binary decision diagrams, ” Computer-Aided Design. ICCAD-93. Digest of Technical Papers, IEEE/ACM International Conference, Pages: 42-47, 1993.
[11] Scholl, C.; Moller, D.; Molitor, P.; Drechsler, R., ” BDD minimization using symmetries, ” Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions, Vol. 18, Pages: 81-100, Feb 1999.
[12] S. Panda.; F. Somenzi, ” Who are the variable in your neighborhood, ” Computer-Aided Design. ICCAD-95. Digest of Technical Papers, IEEE/ACM International Conference, Pages: 74-77, Nov 1995.
[13] S.-W. Jeong, T.-S. Kim, and F. Somenzi, “ An efficient method for optimal BDD ordering computation, ” in Proc. Int. Conf. VLSI and CAD. 1993.
[14] S. J. Friedman and K. J. Supowit, “ Finding the optimal variable ordering for binary decision diagrams, ” IEEE Trans. Comput, Pages: 710-713, May 1990.
[15] T. Shiple, R. Hojati, A. Sangiovanni-Vincentelli, and R. Brayton, ” Heuristic minimization of BDD ’ s using don ’ t cares, ” Design Automation Conf, Pages: 225-231, 1994.
[16] William Hung, Adnan Aziz, and Ken McMillan, ” Heuristic Symmetry Reduction for Invariant Verification, ” International Workshop on Logic Synthesis, Tahoe City, CA. 1997