

Variable Ordering Optimization for OBDD

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ABSTRACT

OBDD (Ordered binary decision diagrams) is the most popular data structure for Boolean function representation in modern logic synthesis/verification EDA tools. It is obvious that the variable ordering is the key factor for reducing the size (nodes) of an OBDD. Therefore, how to find an effective variable order is the most critical issue during OBDD construction. Observing the constructed OBDD of a given variable order, we find that the number of nodes of the OBDD is proportional to the number of branches of the OBDD. Based on this observation, we propose an algorithm for deciding the variable order based on the 0/1 difference between the variables. Experimental results on LGSYNTH 93 benchmark circuits show that our approach is very effective for determining the variable order to reduce the size of OBDD.

Keywords : variable ordering ; ROBDD ; logic synthesis ; VLSI/CAD

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