

OBDD的變數次序優化問題之探討

張世龍、林浩仁

E-mail: 9314763@mail.dyu.edu.tw

摘要

OBDD (Ordered binary decision diagrams)已被廣泛地運用為布林函式的表示方式，是目前布林函式化簡(合成)、驗證等相關VLSI/CAD軟體常使用的布林函式的資料結構。由於變數次序會明顯影響所建構之OBDD的大小(節點個數)，因此，如何決定建構OBDD時的變數順序，是一個重要的議題。經由觀察OBDD所建構出來的樹，我們發現OBDD樹的分支和節點數的增加有相當大的關係。在這篇論文中，我們根據這項發現，依據布林函式中變數之間的關聯，找出規則來調整變數排列順序，將分支較少的變數節點放在較上層，而分支較多的變數節點放在較下層，來降低整體OBDD的節點數。最後以LGSYNTH 93 benchmark circuits為例，與scatter、sifting等方法相來比較。

關鍵詞：OBDD變數次序；ROBDD；邏輯合成；VLSI電腦輔助設計

目錄

封面內頁 簽名頁 授權書.....	iii	中文摘要.....	iv
.....iv 英文摘要.....	v	誌謝.....	vi
.....vi 目錄.....	vii	圖目錄.....	viii
.....ix 表目錄.....	x	第一章 緒論.....	1
第二章 相關研究.....	4	2.1 Bryant的布林函式圖形表示法.....	4
2.2 Friedman與Supowit的演算法.....	4	2.3 Ishiura、Sawada與Yajima的演算法.....	5
2.4 Rudell的篩選(Sifting)演算法.....	5	2.5 Jeong、Kim和Somenzi演算法.....	7
2.6 Panda和Somenzi的研究.....	7	2.7 Bolling、Lobbing和Wegener的研究.....	7
2.8 Scholl、Moller與Molitor的研究.....	8	2.9 Hung、Xiaoyu、Aboulhamid和Driscoll的研究.....	8
第三章 以0/1差異度為基礎的OBDD變數次序演算法.....	9	第四章 實驗及結果分析.....	17
第五章 結論.....	22	參考文獻.....	23
附錄A 布林函式的圖形表示法.....	26	附錄B BDD的簡化規則.....	28
附錄C 相關名詞與符號.....	30	圖1.1 變數次序與BDD大小的影響.....	2
圖2.1 Sifting 演算法變數交換過程.....	6	圖3.1 分支與節點數目的關聯.....	9
圖3.2 函式卡諾圖.....	11	圖3.3 函式卡諾圖.....	14
圖B.1 省略規則.....	28	圖B.2 合併規則.....	29
表3.1 函式 真值表.....	10	表3.2 函式 真值表.....	13
表3.2 扣除變數A之後的真值表.....	15	表3.2 扣除變數A和變數D之後的真值表.....	16
表4.1 差異度演算法.....	19	表4.2 不同演算法間的簡化結果比較.....	20
表4.3 不同演算法的CPU時間(in sec.)花費比較.....	21		

參考文獻

- [1] Bollig, B.; Wegener, I., "Improving the variable ordering of OBDD 's is NP-complete," IEEE Transactions, Vol. 45, Pages: 993-1002, Sep 1996.
- [2] B. Bolling, M. Lobbing, and I. Wegener, "On the effect of local changes in the variable ordering of ordered decision diagrams," Inform. Processing Lett., vol. 59, Pages: 233-239, Oct 1996.
- [3] C. Scholl, D. Moller, and P. Molitor, "BDD minimization Using Symmetries," IEEE Trans. Computer-Aided Designs of Integrated Circuits and Systems, vol. 18, Feb 1999.
- [4] D. Moller and R. Drechsler, "Symmetry based variable ordering for ROBDD 's," in Proc. IFIP Workshop on Logic and Architecture Synthesis, Pages: 47-53, Dec 1994.
- [5] William Hung, Adnan Aziz, and Ken McMillan, "Heuristic Symmetry Reduction for Invariant Verification," International Workshop on Logic Synthesis, Tahoe City, CA.1997.
- [6] Hung, W.N.N.; Xiaoyu Song; Aboulhamid, E.M.; Driscoll, M.A., "BDD minimization by scatter search," Computer-Aided Design of

Integrated Circuits and Systems, IEEE Transactions, Vol. 21, Pages:974-979, Aug 2002.

- [7] N. Zhuang, M.S.T. Bente, P.Y.K. Cheung, "Improved Variable Ordering of BDDs with Novel Genetic Algorithm," IEEE International Symposiums on Circuits and Systems, Atlanta May 1996.
- [8] N. Ishiura, H. Sawada, and S. Yajima, " Minimization of binary decision diagrams based on exchange of variables, " in Proc. Int. Conf. Computer-Aided Design, Pages: 472-475, Nov 1991.
- [9] R.E. Bryant, " Graph-Based Algorithm for Boolean Function Manipulation, " IEEE Trans. Computers, vol. 35, no. 8, Pages: 677-691, 1986.
- [10] Rudell, R., " Dynamic variable ordering for ordered binary decision diagrams, " Computer-Aided Design. ICCAD-93. Digest of Technical Papers, IEEE/ACM International Conference, Pages: 42-47, 1993.
- [11] Scholl, C.; Moller, D.; Molitor, P.; Drechsler, R., " BDD minimization using symmetries, " Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions, Vol. 18, Pages: 81-100, Feb 1999.
- [12] S. Panda.; F. Somenzi, " Who are the variable in your neighborhood, " Computer-Aided Design. ICCAD-95. Digest of Technical Papers, IEEE/ACM International Conference, Pages: 74-77, Nov 1995.
- [13] S.-W. Jeong, T.-S. Kim, and F. Somenzi, " An efficient method for optimal BDD ordering computation, " in Proc. Int. Conf. VLSI and CAD. 1993.
- [14] S. J. Friedman and K. J. Supowit, " Finding the optimal variable ordering for binary decision diagrams, " IEEE Trans. Comput, Pages: 710-713, May 1990.
- [15] T. Shiple, R. Hojati, A. Sangiovanni-Vincentelli, and R. Brayton, " Heuristic minimization of BDD ' s using don ' t cares, " Design Automation Conf, Pages: 225-231, 1994.
- [16] William Hung, Adnan Aziz, and Ken McMillan, " Heuristic Symmetry Reduction for Invariant Verification, " International Workshop on Logic Synthesis, Tahoe City, CA. 1997