A Gridless Channel Router with the Consideration of Crosstalk

陳漢宗、程仲勝

E-mail: 9223678@mail.dyu.edu.tw

ABSTRACT

The interconnection spacing in a VLSI chip becomes denser as the VLSI fabrication technology rapidly evolves. This makes the effect of crosstalks on performance and even on yield in VLSI design and manufacturing increase. The increase of crosstalk will lead to circuit unexpceted circuit behavior and decrease of yield. Consequently, reduction of crosstalks between interconnection wires becomes more and more important in today''s VLSI design. In usage, wires and vias must be placed on tracks and column in grided channel routing. But the same distance between two wires can not use the chip area effectively, so it is unfavorable for crosstalk reduction.In this paper, we propose an algorithm for gridless channel router with crosstalk reduction effectively. In this kind router, the space between two nets are variable. Placing nets according to the weighted constraint graph, a weight in the graph means the distance between two nets. We can calculate crosstalk in each net by built graph. When a net needs to reduce crosstalk, we can increase the distance between another nets. In the graph, it means increase the weight in a edge. In experimental results, the parameters of a channel are given. After all nets are placed by this algorithm, the crosstalk of each net is smaller than crosstalk constraint. The height are close to the height without crosstalk consideration.

Keywords : crosstalk ; gridless channel routing ; weighted constraint graph

Table of Contents

REFERENCES

[01] Naveed A. Sherwani, "Algorithms for VLSI Physical design automation," Kluwer Academic Publishers, 1999.

[02] H. B. Bakoglu , "Circuits, Interconnections and Packaging for VLSI", Addison-Wesley, 1990 [03] M. Burstein and R. Pelavin, "Hierarchical channel router, " Integration VLSI J., vol. 1, pp.21-38, 1983.

[04] C. Y. Roger Chen, Cliff Y. Hou and U. Singh, "Optimal algorithms for bubble sort based on non-Manhattan channel routing, " IEEE Trans. Computer Aided Design, vol. 13, pp. 603-609, 1994.

[05] H. H. Chen and C.K. Wong, "Wiring and Crosstalk Avoidance in Multi-Chip Module Design, " Proc. Custom Integrated Circuits Conference, 1992, pp.28.6.1-28.6.4.

[06] H. H. Chen and E.S. Kuh, "Glitter: A gridless variable-width channel router, " IEEE Trans. Computer Aided Design, vol. CAD-5,pp.459-465,1986.

[07] J. D. Cho and M. S. Chang, "LEXA: A Left-Edge based Crosstalk-Minimum k-color Permutation VHV Channels, " IEEE International Symposium on Circuits and Systems, vol. 3. pp.1704-1704,1997.

[08] J. S. Cherng, S. J. Chen and J. M. Ho, "Crosstalk Minimization in river Routing, " The 8th VLSI Design/CAD Symposium, pp. 265-268, 1997.

[09] K. Chaudhary, A. Onozawa and Ernest S. Kuh, "A spacing algorithm for performance enhancement and crosstalk reduction, " Proc. IEEE/ACM International Conference on Computer Aided Design, pp. 697-702, 1993.

[10] U. Choudhury and A. Sangiovanni- Vincentelli, "Constrained- Based Channel Routing for Analog and Mixed Analog/Digital Circuits, " IEEE International Conference on Computer Aided Design, pp. 195-201, 1990.
[11] David. N, Deutsch, "A dogleg channel router," in Proc. 13th Design Automation Conf., 1976, pp. 425-433.
[12] W. M. Dai, Kong, J. Jue, and M. Sato, "Rubber band routing and dynamic data representation, " Proc. Int. Conf. Computer Aided Design, 1990, pp.52-55.
[13] K. S. Jhang, S. Ha and C. S. Jhon, "COP: A Crosstalk Optimizer for Gridded Channel Routing, " IEEE Trans. Computer Aided Design, vol. 15, no. 4, pp 424-429, Aprial 1996.
[14] T. Gao and C. L. Liu, "Minimum Crosstalk Channel Routing, " IEEE Trans. Computer Aid Design, Vol. 15, no 5, pp. 465-474, May 1996.
[15] T. Gao and C. L. Liu, "Minimum Crosstalk Switch-box Routing, "Proc. ICCAD, pp.610-615, 1994.
[16] D. Hee Il Ahn, Seung Kee Han, Tae Won Cho, "Genrouter : A Genetic Algorithm for Channel Routing Problems", IEEE, pp.151-154, 1995
[17] D. Hightower, "A generalized channel router, " in Proc. 17th Design Automation Conf., 1980, pp22-31.
[18] I. Harada, H. Kitajawa and T. Kaneko, "A Routing System for Mixed A/D Standard Cell LSI's, " IEEE International Conference on Computer Aided Design, pp. 378-381, 1990.
[19] Kuo-Chin Hsu, Yu-Chung Lin, Po-Xun Chiu, and Tsai-Ming Hsieh, "Minimum Crosstalk Channel Routing with Dogleg, " to appear IEEE International Symposium on Circuit and Systems, 2000.
[20] T. T. Ho, S. S. Iyengar, and S. Q. Zheng, "A general greedy channel routing algorithm, " IEEE Trans. Computer Aided Design, vol. 10, pp. 204-211, Feb. 1991.
[21] D. Kirkpatrick, A. L. Sangiovanni-Vicentelli, "Techniques for Crosstalk Avoidance in the Physical Design of High-Performance Digital Systems, " Interational Conference on Compuer Aided Design, pp. 616-619, 1994.
[22] S. Kirpatrick, C. D. Gelatt Jr. and M. P. Vecchi, "Optimization by Simulated-Annealing, " Science, Vol 220, pp. 671-680, 1983.
[23] J. Lienig and K. Thulasiraman, "A New Genetic Algorithm for the Channel Routing Problem, " Proceedings of the Seventh International Conference on VLSI Design, pp.133-136, 1994.
[24] A. Onzawa, K. Chaudhary and E. S. Kuh, "Performance Driven Spacing Algorithm Using Attractive and Repulsive Constraints for Submicron LSI's, " IEEE Trans. Computer Aided Design, Jun. 1995, vol. 14, no. 6, pp. 707-719.
[25] A. Sangiovanni-Vincentelli, M. Santomauro et al., "A new gridless router: Yet another channel router (YACR-II), " Proc. Int. Conf. Computer Aided Design, 1984, pp. 72-75.
[26] H. Shin, A. Sangiovanni-Vincentelli, "A detailed router based on incremental routing modification: Mighty, " IEEE Trans. Computer Aided Design, vol. 6, pp. 942-955, Nov. 1987.
[27] K. Sato et al., "A 'grid-free' channel router, " in Proc. 17th Design Automation Conf., 1980, 22-31 [28] P. Saxena and C.L. Liu, "Crosstalk Minmization using Wire Perturbation, " DAC, 1999, pp. 100-103.
[29] T. Sakuri and K. Tamaru, "Simple formulas for two and three dimensional capacitance, " IEEE Transaction on Electronic Devices, 70:183-185, 1983.
[30] Thomas G. Szymanski, "Dogleg channel routing is NP- COMPLETE, " IEEE Trans. Computer Aided Design, vol. CAD-4, pp. 31-40, Jan. 1985.
[31] S. Thakur, K.Y. Chao and D.F. Wong, "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three Layer VHV Channel Routing, " Proc. IEEE International Symposium on Circuits and System, 1995, pp. 207-210.
[32] T. Xue, E. S. Kuh and D. Wang, "Post Global Routing Crosstalk Risk Estimation and Reduction, " International Conference on Computer Aided Design, pp. 302-309, 1996.
[33] Jin-Tai Yan, "Optimal Routing Ordering and Layer Assignment for Via Minimization in Bubble-Sorting-Based Non-Manhattan Channel, " The 9th VLSI Design/CAD Symposium, 1998, pp. 351-354.
[34] T. Yoshimura and E. S. Kuh, "Efficient algorithms for channel routing, " IEEE Trans. Computer-Aided Design, vol. CAD-1, no.1, pp 25-35, Jan. 1982 [35] H. Zhou and D. F. Wong, "An Optimal Algorithm for River Routing with Crosstalk Constraints, " IEEE/ACM International Conference on Computer Aided Design, 1996.
[36] H. Zhou and D. F. Wong, "Crosstalk-Constrained Maze Routing Based on Lagrangian Relaxation, " IEEE International Conference on Compuer Design, pp. 628-633, 1997.
[37] H. Zhou and D. F. Wong, "Global Routing with Crosstalk Constraints, " Proc. Design Autom. Conf., 1998, pp. 374-377.