A Congestion-Driven Post-Floorplanner

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ABSTRACT

ABSTRACT As VLSI technology progresses, the design complexity, the integration degree, and the routing density increase rapidly. Therefore, the estimation of routing congestion before routing phase is one of most important issues in today ’ s VLSI physical design. Floorplanning is an important phase in the VLSI physical design. In this paper, we propose a congestion-driven post-floorplanner for reducing the routing congestion. Besides considering chip area optimation, the proposed floorplanner can minimize wire length and reduce routing density under good area control. In our approach, an initial floorplan of a chip represented by a slicing tree is given. Currently, the initial floorplan is constructed by using the method proposed by F. Y. Young and D. F. Wong and its area is bounded by 5/4 of the total areas of all modules. For the initial floorplan, the interconnection length of each net and the routing density of each routing region can be calculated for evaluating the degree of noise within chip. Then the initial floorplan is transformed into the corresponding slicing tree in which leaf nodes represent soft modules and internal nodes represent cut ways. For the slicing tree, the proposed post-floorplanner adopts a top-down tree search method and a pairwise module interchange strategy to locally improve the initial floorplan and reduce routing congestion within the chip. The experimental results show that the proposed post-floorplanner can generate, on average, 18.36% and 31.15% improvements for the wire length and routing density, respectively.

Keywords : Floorplanning ; Physical design ; Congestion

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