以繞線擁擠程度為導向之後置平面規劃器

吳彬玄、程仲勝

E-mail: 9223486@mail.dyu.edu.tw

摘 要

中文摘要 隨著VLSI製程技術日益進步，設計複雜度增加，晶片整合程度和線路密度的大幅提昇，導致干擾日益嚴重，若控制不當，必定會影響晶片系統效能而影響產能。因此如何在後端實體設計(physical design)階段考慮繞線擁擠(congestion)程度已是刻不容緩的事。 平面規劃(floorplanning)是VLSI實體設計相當重要的一環，因此本篇論文提出一個以降低繞線擁擠程度(congestion)為導向的軟性模組(soft module)平面規劃器(floorplanner)。除了將晶片面積做最佳化之外，所提平面規劃器更可在面積不增加的情況下對可能導致嚴重時序(timing)延遲的較長連接線與可能導致嚴重繞線擁擠程度的高繞線密度區域做最佳化處理，以減少晶片內干擾的程度。 在我們的方法中，為了控制晶片面積，首先採用F. Y. Young與D. F. Wong所提出之演算法以產生面積不大於總模組面積5/4的可切割平面圖(slicing floorplan)為初始平面圖，並對此初始平面圖計算出各網列連線長度和各區域繞線密度，以評估晶片內的干擾程度；接著將此初始平面圖轉換成一個可切割樹狀結構(slicing tree)，其中樹葉節點表示軟性模組，內部節點表示切割方式，並採用一個由上到下(top-down)的樹狀結構搜尋策略和模組兩兩交換策略，漸進的局部改進平面圖以達到降低晶片內繞線長度及擁擠的程度。 經由實驗的結果顯示，我們所提出的後置平面規劃演算法，在晶片面積不增大的情況下，平均而言，網列連線長度可以改進18.36%，繞線密度可以改進31.15%，因此能有效的控制連線長度與擁擠程度所造成的干擾。

關鍵詞 : 平面規劃 ; 實體設計 ; 擁擠程度

目錄

參考文獻

參考文獻 [1] Yun-Chih Chang, Yao-Wen Chang, Guang-Ming Wu and Shu-Wei Wu,“ B*-trees: a new representation for nonslicing floorplans, ” Proc. Design Automation Conf., pp. 458-463, 2000.

[2] Hung-Ming Chen, Hai Zhou, F.Y. Young, D.F. Wong, H.H. Yang and N.Sherwani,“ Integrated floorplanning and interconnect planning, ” Proc. ICCAD, pp. 354-357, 1999.

[3] Jason Cong, Tianming Kong and D.Z. Pan“ Buffer block planning for interconnect-driven floorplanning, ” Proc. ICCAD, pp. 358-363, 1999.

[4] P. N. Guo, C. K. Cheng, and T. Yoshimura,“ An O-tree Representation of Non-Slicing Floorplan and Its Application, ” Proc. Design Automation Conf., pp. 268-273, 1999.

[5] L. P. P. P. van Ginneken and R. H. J. M. Otten,“ Optimal slicing of plane point placements, ” Proc. Int. Conf. Computer Design, pp. 328-334, 2001.

[6] Pei-Ning Guo, T. Takahashi, Chung-Kuan Cheng and T. Yoshimura,“ Floorplan using a tree representation, ” IEEE Trans. On Comp. Aided Design of IC ’ s and System, Vol.20, NO.2, pp. 281-289, Feb 2001.

[7] Xianlong Hong, Sheqin Dong, Gang Huang, Yuchun Ma, Yici Cai, Chung-Kuan Cheng, Jun Gu,“ A non-slicing floorplanning algorithm using corner block list topological representation, ” IEEE APCCAS, pp. 833-836, 2000.

[8] K. Kiyota and K. Fujiyoshi,“ Simulated annealing search through general structure floorplans using sequence-pair, ” in Proc. Circuits and Systems, Vol.3, pp. 77-80, 2000.

[9] M. Lai and D. F. Wong,“ Slicing tree is a complete floorplan representation, ” in Proc. Design Automation and Test in Europe Conf.,

pp.228-232, 2001.
[10] D. P. Lapotin and S. W. Director, “ A global floor-planning tool, ” Proc. ICCAD, pp. 143-145, 1985.
[11] S. C. Lee, J. M. Hsu, and Y. W. Chang, “ Multilevel large-scale module placement/floorplanning using B*-trees, ” Proc. of the 12th VLSI Design/CAD Symposium, Hsinchu, Taiwan, Aug. 2001.
[12] J. M. Lin and Y. W. Chang, “ TCG: A Transitive Closure Graph-Based Representation for Non-Slicing Floorplans, ” Proc. Design Automation Conf., pp. 764-769,2001.
[13] J. M. Lin, and Y. W. Chang, “ A P-admissible non-slicing floorplan representation with a worst-case linear-time packing scheme, ” Proc. The 12th VLSI Design/CAD Symposium, Hsinchu, Taiwan, Aug. 2001.
[14] H. Murata, K. Fujiyoshi, S. Nakatake, and Y. Kajitani, “ Rectangle-Packing-Based Module Placement, ” Proc. ICCAD, pp. 472-479, 1995.
[15] H. Murata, K. Fujiyoshi, S. Nakatake, and Y. Kajitani, “ VLSI Module Placement base on Rectangle-Packing by The Sequence Pair, ” IEEE Trans. Computer-Aided Design, Vol. 15, pp. 1518-1524, 1996.
[16] H. Murata and E. S. Kuh, “ Sequence-Pair Based Placement Method for Hard/Soft/Pre-placed Modules, ” Proc. ISPD, pp. 167-172, Apr. 1998.
[17] S. Nakatake, K. Fujiyoshi, H. Murata and Y. Kajitani, “ Module Placement on BSG-Structure and IC Layout Applications, ” Proc. ICCAD, pp. 484-491, 1996.
[18] T. Ohmura, K. Fujiyoshi, and C. Kodama, “ Area optimization of packing represented by sequence-pair, ” in Proc. Circuits and Systems Conf., pp. 813-816, 2000.
[19] R. H. J. M Otten, “ Automatic Floorplan Design, ” Proc. Design Automation Conf., pp 261-267, 1992.
[20] R. H. J. M Otten, “ Efficient floorplan optimization ” IEEE international Conference on Computer Desing, pp 499-502, 1983.
[21] A. Ranjan, K. Bazargan, and M. Sarrafzadeh, “ Floorplanner 1000 Times Faster: A Good Predictor and Constructor, ” In System Level Interconnect Prediction, pp. 115-120, 1999.
[22] A. Ranjan, K. Bazargan, and M. Sarrafzadeh, “ fast Hierarchical floorplanning with congestion and timing control, ” Proc. ICCD, pp. 357-362, 2000.
[23] A Ranjan, K. Bazargan, S. Ogrenci, and M. Sarrafzadeh, “ Fast Floorplanning for Effective Prediction and Constructor, ” IEEE Transactions on VLSI System, Vol.9, No.2, pp. 341-351, April 2001.
[24] D. F. Wong and C. L. Liu, “ A New Algorithm for Floorplan Design, ” Proc. Design Automation Conf., 1986.
[25] D. F. Wong and T. Xiaoping, “ FAST-SP: a fast algorithm for block placement based on sequence pair, ” Proc. Design Automation Conf., pp521-526,2001.
[26] G. M. Wu, Y. C. Chang, and Y. W. Chang, “ Rectilinear Block Placement Using B*-trees, ” Proc. ICCD, pp. 351-356, Austin, TX, Oct. 2000.
[27] T. Xiaoping, T. Ruiqi, and D. F. Wong, “ Fast evaluation of sequence pair in block placement by longest common subsequence computation, ” IEEE Transaction Computer-Aided Design of Integrated Circuits and Systems, Vol.20, No.12, pp. 1406-1413, 2001.
[28] F. Y. Young and D. F. Wong, “ How Good Are Slicing Floorplan ?, ” ACM International Symposium on Physical Design, 1997.
[29] F. Y. Young and D. F. Wong, “ Slicing Floorplans with Pre-place Modules, ” Proc. IEEE international Conf. On Computer-Aided Design, pp. 252-258, 1998.
[30] F. Y. Young, D. F. Wong, and Hannah H. Yang, “ Slicing Floorplan with Range Constraint, ” IEEE Transactions on CAD of Integrated Circuits and Systems, Vol. 19, NO. 2, February, pp. 272-278, 2000.