A Study on CMOS RF Front-End LNA Circuit

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ABSTRACT

A CMOS Low Noise Amplifier (LNA) which is suitable for Radio Frequency (RF) wireless applications will be investigated in this paper. A fully integrated 2.38-GHz CMOS LNA implemented by using 0.25 μ m CMOS technology with 2.5V power supply. The main simulation points are input/output impedance matching, isolation, power gain, linearity and power consumption. Through adjusting the component values of LNA, we can find out the optimization of LNA. Simulation results show that the LNA has the features of power gain of 20dB, noise figure of 1.5dB, IP3 of -18dBm, power dissipation of 18.5mW, and well-matched input/output.

Keywords : CMOS LNA ; wireless ; fully integrated amplifier ; low noise ; noise figure ; 1-dB compression ; IP3

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