Testing and Diagnosis Methodology for FPGA

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ABSTRACT

In this thesis, we study the testing and fault diagnosis techniques for the CLBs and internal interconnect of an FPGA. We expect to improve or make any contribution to those techniques in the feature. With respect to testing the CLBs, the AND/OR-tree approach [5] is C-testable and can detect multiple faulty CLBs. Besides, the number of required I/O block is less. We take Xilinx Spartan FPGA as an example and use the single S-A-0(1) fault model, to illustrate how to use Y. Zorian's test strategy [13] to generate minimum test configurations and test sequence for the single CLB. The AND/OR-tree approach is used to compare and deliver the output response. With respect to the CLB fault diagnosis, we use several horizontal and vertical MAJ-trees to locate any single faulty CLB and all possibly faulty CLBs under multiple faulty CLBs. Then, we use the Naive approach [5] to locate all multiple faulty CLBs. With respects of interconnect test and fault diagnosis, we introduce Y. Zorian's test configurations [17] and Yinlei Yu's fault diagnosis approach [22] to illustrate how to test and diagnose the two-dimensional array of switch matrixes.

Keywords : FPGA ; interconnect ; CLB ; test ; fault diagnosis

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