# 微影製程之疊對回授控制

**劉德庠、陳俊達 ; 張耀仁**

E-mail: 9222161@mail.dyu.edu.tw

**ABSTRACT**

According to the demand of field transformation recently, the semiconductor has become one of the main field in Taiwan, and the improvement of fabrication processes is necessary to progress. The technology of Lithography is more important when the Critical Dimension is getting smaller. Any positioning mismatch between layers during exposure process results in overlay error. Firstly, it can be divided into Interfield and Intrafield to explore the resource of overlay error in this research, and to analyze reasons and physical-meaning are caused by each error coefficient. Some researchers have examined the parameters of overlay error by the method of least square. However, the controllable order terms can affect to accuracy of the parameter estimation if only the uncontrollable order terms as considered. Therefore, the method of this research is that the model of overlay error can be discussed two parts: controllable parameters and uncontrollable parameters. The Lagrange method is then utilized to find out the maximum of uncontrollable parameters. In other words, the possibly maximal inherent equipment error is calculated. Finally, the data collected from the measuring machine in the practical experiment apply to the practical example in order to count the value of parameter of an area and whole area. Through the comparison between both to understand the exposuring situation of whole wafer, that can enhance the judgement of engineers and also reach the goal of improving the process quality, raising the efficiency of overall equipment.

Keywords : Overlay error ; Least square ; Lagrange

**Table of Contents**

封面內頁 簽 名 頁 授權書...........................................iii 中文摘要.........................................v 英文摘要.........................................vi 誌謝............................................viii 目錄............................................ix 圖目錄...........................................xi 表目錄..........................................xiii 第一章 序論 1.1 研究動機與目的................................1 1.2 文獻回顧.....................................2 1.3 研究方法.....................................3 1.4 論文架構.....................................4 第二章 微影製程與疊對誤差介紹 2.1 微影製程介紹..................................5 2.2 疊對誤差模式.................................15 第三章 研究方法 3.1 系統未知參數估測理論..........................19 3.2 研究方法之推導...............................21 3.2 參數估算之流程...............................26 第四章 模擬結果與實際應用 4.1 數值模擬結果................................ 29 4.2 實際應用結果.................................32 第五章 結論 5.1 綜合結論.....................................48 5.2 未來方向與展望...............................49

**REFERENCES**

1] Michael Quirk and Julian Serda, "Semiconductor Mnufacturing Technology, " pp.355-471, 2001.

[2] Christopher Gould, "Advanced Process Control:Basic Functionality Requirements for Lithography, " IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 2001.

[3] Perioff , D.S., "A Four-Point Electrical Measurement Technique for Characterizing Mask Superposition Errors on Semiconductor Wafer," IEEE Journal of Solid-State Circuits, Vol.SC-13, No.4, pp.436-444 , Augst, 1978.

[4] MacMillen, D.and W.D.Ryden, "Analysis of image field placement deviations of a 5*microlithography reduction lens," Proceedings SPIE: Optical Micro-Lithography- Technology, Vol.334, PP.78-89, 1982.

[5] C. K. Peski, "Minimizing Patter Registration Error Through Wafer Stepper Matching Techniques," Solid State Technology, pp.111-115, May 1982.

[6] Fink, I., Neal Sullivan and James, S. Leaks, "Overlay Sample Plan Optimization for the Detection of Higher Order Contributions to Mislignment, " SPIE Vol.2196 ,Integrated Circuit Metrology, Inspection, and process Control, VIII, pp.389-399, 1994.

[7] Stauch, H., K.Simon, H.-V. Scheunemann and H.-L. Huber, "Impact of Chuck Flatness on Wafer Distortion and Stepper Overlay-Comparison of Experimental and FEM-Results, " Microelectronic Engineering 23, pp.197-201, 1994.

[8] Warren W.Flack, Gary E. Flores, Alan Walther and Manny Ferreira " A Reticle Correction Technique to Minimize Lens Distortion Effects, " BACUS Symposium, 1994.

[9] Zone-Ching LIN and Wen-Jang WU, "Multiple Linear Regression Analysis of the Overlay Accuracy Model, " IEE,Vol.12, NO.2, May 1999.

[10] Zone-Ching LIN and Wen-Jang WU, "Analysis of Overlay Accuracy Error Parameters, " Proc.Natl.Sci.Counc.ROC Vol.22 NO2, PP.261-271, 1998.
[11] D. Jian, M. Zhang "Yield Improvement Research on Modeling Overlay Error & Sampling Strategies," 2000.
[12] 郭政達, "LEICA EBML300電子束直寫對準原理及記號辨識簡介", 奈 米通訊, 2003.
[13] 陳俊淇、范瑞雲、柯富祥," I-Line Stepper對準效率與曝光平 台之關係", 奈米通訊, 2003.
[14] 莊達仁, "VLSI製造技術", 高利圖書有限公司, 2002.
[15] 張勁燕, "半導體製成設備", 伍南圖書.
[16] 李文猶、劉俊宏、蔡嘉鴻、楊朝全, "半導體Overlay量測機 台之參數收集與分析系統", 機械工業雜誌, 2002/9, 234期.
[17] M. van den Brink, C. de Mol and R. George, "Matching Performance for Multiple Wafer Steppers Using an Advanced Metrology Procedure, " Proceeding SPIE 921: Integrated Circuit Metrology, Inspection and Process Control II, 1988.
[18] W. H. Arnold, "Image placement differences between 1:1 projection aligners and 10:1 reduction wafer steppers, " Proceedings SPIE: Opt. Microlith., Vol.394, pp.87-98, 1983.
[19] J. Armitage, "Analysis of Overlay Distortion Patterns, " Proceedings SPIE 921:Integrated Circuit Metrology Inspection and Process Control II, 1988.
[20] M. van den Brink, C. de Mol and R. George, "Matching Performance for Multiple Wafer Steppers Using an Advanced Metrology Procedure, " Proceedings SPIE 921:Integrated Circuit Metrology Inspection and Process Control II, 1988.
[21] Karl Johan Astrom Bjorn,"Adaptive Control",pp.43-55 [22] 方崇智、蕭德云, "過程辨識", 儒林.
[23] 趙清風, "控制之系統識別", 全華.
[24] 韓增晉, "適應控制系統", 科技圖書股份有限公司.
[25] Papila, M. and Haftka, R. T., "Uncertainty and Response Surface Approximations, " 42nd AIAA/ASME/ASCE/ASC Structures, Structural Dynamics, and Material Conference, Paper AIAA-01-1680, Seattle, WA, April 2001.
[26] Papila, M., Papila N., Shyy, W., Haftka, R. T. and Fitz- coy, N. "Error-based Design Space Windowing, " 40th AIAA mAerospace Sciences Meeting and Exhibit, Paper AIAA-02- 0539, Reno, Nevada, January, 2002.
[27] Myers, R. H., and Montgomery, D. C., "Response Surface Methodology Process and Product Optimization Using Designed Experiments, " New York: John Wiley & Sons, Inc., pp.208-279, 1995.