利用基因演算法解決通道繞線上串音問題

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摘 要

隨著VLSI製程技術的日益精進，在VLSI晶片中內部連接線之間的距離變的越來越緊密，這使得連線間 的串音(CROSSTALK)問題越來越嚴重，進而影響VLSI晶片效能與其良產率（YIELD）。由於串音的增加將 會造成電路訊號傳遞的延遲(SIGNAL DELAY)並且導致電路行為的不穩定，甚至造成良產率的降低。因此 ，減少連接線間的串音值在今日的VLSI設計中變的非常重要。 在本論文中，我們提出一個在格子化(GRID-BASED)的通道繞線問題中能夠降低串音的方法稱之為GACR (GENETIC ALGORITHM CROSSTALK REDUCTION)演算法。我們的方法主要是以基因演算法(GENETIC ALGORI -THM)為基礎所發展出來的，並且利用基因演算法中選擇(SELECTION)、交配(CROSSOVER)以及突變(MUTA -TION)等基本運算子的重複運算來達到串音最小化的結果。由實驗結果得知，我們所得到的結果與先前 的研究作比較，我們的方法均優於或近似於先前的方法。

關鍵詞 : 串音，通道繞線，基因演算法

目錄

參考文獻

[1]H. B. BAKOGLU, "CIRCUITS INTERCONNECTIONS AND PACKAGING FOR VLSI," ADDISON-WESLEY,1990.
[2]T. GAO AND C. L. LIU, "MINIMUM CROSSTALK CHANNEL ROUTING," IEEE TRANS. COMPUTER AID DE -SIGN, VOL. 15, NO 5, PP. 465-474, MAY 1996.
[3]T. GAO AND C .L. LIU, "MINIMUM CROSSTALK SWITCH-BOX ROUTING," IEEE/ACM INTERNATIONAL C -ONFERENCE ON. COMPUTER AID DESIGN, 1994, PP. 610-615.
[4]K. S. JHANG, S. HA AND C. S. JHON, "COP: A CROSSTALK OPTIMIZER FOR GRIDDED CHANNEL ROU -ING, " IEEE TRANS. COMPUTER AIDED DESIGN, VOL. 15, NO. 4, PP. 424-429, APRIL 1996.
[5]S. THAKUR, K. Y. CHAO AND D. F. WONG, "AN OPTIMAL LAYER ASSIGNMENT ALGORITHM FOR MINIM -IZING CROSSTALK FOR THREE LAYER VHV CHANNEL ROUTING," PROC. IEEE INTERNATIONAL SYMPOS -IUM ON CIRCUITS AND SYSTEM, 1995, PP. 207-210.
[6]K. CHAUDHARY,A. ONOZAWA AND E. S. KUH,"A SPACING ALGORITHM FOR PERFORMANCE ENHANCEMENT AND CROSSTALK REDUCTION," PROC.IEEE/ACM NTERNATIONAL CONFERENCE ON.COMPUTER AID DESIGN, 1993, PP. 697-702.
[7]H. H. CHEN AND C. K. WONG, "WIRING AND CROSSTALK AVOIDANCE IN MULTI-CHIP MODULE DESIGN, "PROC. CUSTOM INTEGRATED CIRCUITS CONFERENCE, PP. 28.6.1-28.6.4, 1992.
[8]W. M. DAI, R. KONG, J. JUE AND M. SATO, "RUBBER BAND ROUTING AND DYNAMIC DATA REPRESENT ATION," PROC.INT. CONF. COMPUTER AID DESIGN, PP. 52-55, 1990.
[9]D. KIRKPATRICK, A. L. SANGIOVANNI-VICENTELLI, "TECHNIQUES FOR CROSSTALK AVOIDANCE IN TH -E PHYSICAL DESIGN OF HIGH-PERFORMANCE DIGITAL SYSTEMS, "INTERNATIONAL CONFERENCE ON CO -MPUTER AIDED DESIGN, PP. 616-619, 1994.
[10]A. ONOZAWA, K. CHAUDHARY AND E. S. KUH, "PERFORMANCE DRIVEN SPACING ALGORITHM USING AT -TRACTIVE AND REPULSIVE CONSTRAINT FOR SUBMICRO LSI'S," IEEE TRANS. COMPUTER AIDED DES -IGN, JUN. 1995, VOL. 14, NO. 6, PP-707-719.
[11]T. SAKURAI AND K. TAMARU, "SIMPLE FORMULAS FOR TWO AND THREE DIMENSIONAL CAPACITANCE," IEEE TRANSACTIONS ON ELECTRONIC DEVICES, PP. 183-185, 1993.
[12]T. G. SZYMANSKI, "DOGLEG CHANNEL ROUTING IS NP-COMPLETE," IEEE TRANS.COMPUTER AIDED DE -SIGN, VOL. CAD-4, PP. 31-40, JAN. 1985.
[13]DEUTSCH, D. N. , "DOGLEG CHANNEL ROUTER," PORC. 13TH DESIGN AUTOMATION CONF., PP. 425- 433, 1976.
[14]T. YOSHIMURA AND E. S. KUH, "EFFICIENT ALGORITHM FOR CHANNEL ROUTING," IEEE TRANS.COMP -UTER AIDED DESIGN ICS SYSTEM 1, PP. 25-35, 1982.
[15]R. L. RIVEST AND C. M. FIDUCCIA, "A GREEDY CHANNEL ROUTER," IN PROC.19TH DESIGN AUTOMA -TION CONF., LAS VEGAS, NV, JUNE 1982, PP. 418-424.
[16]M. BURSTEIN AND R. PELAVIN, "HIERARCHICAL CHANNEL ROUTER," INTEGREATION VLSI J. VOL 1, PP. 21-38, 1983.
[17]H. ZHOU AND D. F. WONG, "AN OPTIMAL ALGORITHM FOR RIVER ROUTING WITH CROSSTALK CONSTRA -INTS," IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN, 1996.
[18]J. S. CHERNG, S. J. CHEN AND J. M. HO, "CROSSTALK MINIMIZATION IN RIVER ROUTING," THE 8TH VLSI DESIGN/CAD SYMPOSIUM, PP. 265-268, 1997.
[19]P. SAXENA AND C. L. LIU, "CROSSTALK MINIMIZATION USING WIRE PERTURBATION," DAC, 1999, PP. 100-103.
[20]KUO-CHIN HSU, YU-CHUNG LIN, PO-XUN CHIU, AND TSAI-MING HSIEH, "MINIMUM CROSSTALK CHAN -NEL ROUTING WITH DOGLEG," TO APPEAR IEEE INTERNATIONAL SYMPOSIUM ON CIRCUIT AND SYSTE -MS, 2000.
[21]J. H. HOLLAND, "ADAPTATION IN NATURAL ARTIFICIAL SYSTEMS," UNIVERSITY OF MICHIGAN PRESS, ANN ARBOR. MICH, 1975.
[22]D. E. GOLDBERG, GENETIC ALGORITHMS IN SEARCH, OPTIMIZATION, AND MACHINE LEARNING, READ -ING, MA:

ADDISON-WESLEY, 1989.
[23]A. HASHIMOTO AND J. STEVENS, "WIRE ROUTING BY OPTIMIZATION CHANNEL ASSIGNMENT WITHIN L -ARGE APERTURES," PROCEEDINGS OF 8TH DESIGN AUTOMATION WORKSHOP, PP. 155-163, 1971.
[24]Y. L. LIN, Y. C. HSU AND F. S. TSAI, "SILK: A SIMULATED EVOLUTION ROUTER," IEEE TRANS. COMPUTER AIDED DESIGN. VOL.8, NO. 10, PP. 1108-1114, 1989.
[25]J.LIENIG AND K. THULASIRAMAN,"A NEW GENETIC ALGORITHM FOR THE CHANNEL ROUTING PROBLEM, "PROCEEDINGS OF THE SEVENTH INTERNATIONAL CONFERENCE ON VLSI DESIGN, PP. 133-136,1994 [26]J. LIENIG, "A PARALLEL GENETIC ALGORITHM FOR TWO DETAILED ROUTING PROBLEMS," PROCEED -INGS OF THE 1996 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, ISCAS-96, PP. 508-511, 1996.
[27]B. B. PRAHLADA RAO, L. M. PATNAIK AND R. C. HANSDAH, "A GENETIC ALGORITHM FOR CHANNEL ROUTING USING INTER-CLUSTER MUTATION," SUBMITTED FOR PUBLICATION.
[28]B. B. PRAHLADA RAO, L. M. PATNAIK AND R. C. HANSDAH, "PARALLEL GENETIC ALGORITHM FOR CHANNEL ROUTING PROBLEM," PROC. OF THE IEEE THIRD GREAT LAKE SYMPOSIUM ON VLSI DESIGN, KALAMAZOO, MICHIGAN, MARCH 5-6, 1993, PP. 69-70.
[29]HEE IL AHN, SEUNG KEE HAN, TAE WON CHO, "GENROUTER : A GENETIC ALGORITHM FOR CHANNEL R -OUTING PROBLEMS", IEEE, PP. 151-154, 1995.
[30]N. A. SHERWANI, "ALGORITHM FOR VLSI PHYSICAL DESIGN AUTOMATION, "KLUWER ACADEMIC PUBLI -SHERS.
[31]NOBUO FUNABIKI AND YOSHIYASU TAKEFUJI, "A PARALLEL ALGORITHM FOR CHANNEL ROUTING PROBL -EMS,"IEEE TRANS. OF.CAD, VOL.11, NO. 4, PP. 464-474, 1992.
[32]ANTHONY D. JOHNSON, "A GENETIC ALGORITHM FOR VLSI CHANNEL ROUTING IN THE PRESENCE OF C -YCLIC VERTICAL CONSTRAINTS," IEEE, 1997.
[33]R. JOOBBANI, "AN ARTIFICIAL INTELLIGENCE APPROACH ON VLSI ROUTING," ACADEMIC PUBLISHER -S, 1986.
[34]J. LIENIG AND K. THULASIRAMAN, "A GENETIC ALGORITHM FOR CHANNEL ROUTING IN VLSI CIRCUI -TS", EVOLUTIONARY COMPUTATION, VOL. 1, NO. 4, PP. 293-311, 1994.