以FPGA實現PID 模糊控制晶片之設計

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摘 要

近來，使用微處理器的數位PID 模糊控制系統在工業領域獲得廣泛的應用。為提昇即時多工的處理 速度，需要更加複雜與更高速的運作系統，而這些系統往往採分散式微處理器運作模式。本論文中， 我們研究設計PID 模糊控制硬體晶片。此晶片設計不僅能達到高速推論的需求，更能在複雜環境下， 避免因外部雜訊干擾所產生之故障與錯誤的推論結果，所以可靠度相當良好。在晶片設計過程中，首 先我們使用MATHCAD軟體驗證PID模糊推論，接著以VERILOGHDL（HARDWARE DESCRIPTION LANGUAGE)和 ALTERA FPGA（FIELDPROGROMM- ABLE GATE ARRARY）設計與模擬電路。最後我們使用個人電腦與邏輯 分析儀測試我們的設計。

關鍵詞 : PID、FUZZY、FPGA、智慧型

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