LOW POWER BUS DRIVER CIRCUIT DESIGN

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ABSTRACT

LOW POWER DESIGN IS IMPORTANT DUE TO THE INCREASING DEMAND FOR PORTABLE PRODUCTS AND THE EXPENSIVE COST FOR HEAT DISSIPATION. IN THIS THESIS, ATTENTION HAS BEEN PAID TO REDUCE THE POWER CONSUMPTION OF A HIP WITH LARGE CLOCK/BUS LOAD. GENERALLY, A BUS SYSTEM CONSUMES A TREMENDOUSLY SIGNIFICANT PORTION OF POWER IN THE WHOLE CHIP. IN ORDER TO DECREASE THE DEGREE OF POWER CONSUMPTION, WE LAUNCH A LOW-SWING BUS DRIVER CIRCUIT AS WELL AS A LOW SWI -NG BUS DRIVER CIRCUIT WITH CHARGE RECYCLING TECHNIQUE. A SIGNIFICANT REDUCTION IN POWER DI -SSIPATION IS ACHIEVED, DUE TO THE REDUCED SWING VOLTAGE ON THE INTERCONNECTION LOADS. THE DRIVER CHIP WAS IMPLEMENTED WITH A TSMC 0.35 μ M CMOS PROCESS TECHNOLOGY.

Keywords: BUS DRIVER, LOW-SWING, CHARGE RECYCLING, LOW POWER

Table of Contents

第一章緒論--P1 1.1 動機--P1 1.2 功率消耗的來源--P2 1.3 論文組織--P4 第二章電荷循環使用及降低振盪電壓的簡介--P5 2.1 電荷循環使用(CHARGE RECYCLE)--P6 2.2 降低振盪電壓(VOLTAGE SWING REDUCTION)--P8 第三章匯流排驅動電路--P12 3.1 傳統CMOS 驅動電路--P12 3.2 REDUCED SWING DRIVER-VOLTAGE SENSE TRANSLATOR(RSDVST)--P14 3.3 SYMMETRIC SOURCE-FOLLOWER DRIVER WITH LEVEL CONVERTER(SSDLC)--P16 3.4 LOW SWING LEVEL CONVERTER(LSLC)--P18 3.5 STATIC DRIVER WITH VOLTAGE SENSE TRANSLATOR(SDVST)--P20 3.6 CONVENTIONAL CMOS CIRCUIT WITH CHARGE RECYCLING(CMOSCR)--P22 3.7 LOW SWING LEVEL CONVERTER WITH CHARGE RECYCLING(LSLCCR)--P24 3.8 STATIC DRIVER WITH VST AND CHARGE RECYCLING(SDVSTCR)--P27 3.9 模擬結果與比較--P31 第四章實驗結果--P33 4.1 設計流程--P33 4.2 佈局設計--P34 4.3 實驗結果--P37 4.4 預計規格與實測結果--P39 4.5 討論與結論--P41 第五章結論--P42 參考文獻--P44 附錄--P48

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