低功率匯流排驅動電路之設計

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摘 要

低功率的設計是對於可攜式產品的需求增加和對降低散熱成本的需要。在本文中著重於降低脈衝緩 衝器及匯流排負載晶片的功率消耗。匯流排（BUS）電路的功率消耗佔整個積體電路功率消耗非常大 的份量，為了降低其功率消耗，所以本篇論文提出降低匯流排上的電壓振幅（VOLTAGE SWING）之驅 動電路及結合電荷循環使用（CHARGERECYCLE）技術的驅動電路。由於降低了負載上的電壓振幅，所 以也就大大的減少電路功率的消耗。此電路使用台積電0.35 M M 製程模擬。

關鍵詞 : 匯流排、電壓振幅、電荷循環使用、低功率

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