A STUDY OF ESD PROTECTED CIRCUIT DESIGN AND LATCH UP EFFECT IMMUNITY

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ABSTRACT

FOLLOWING THE INTEGRATED CIRCUIT PACKAGE DENSITY INCREASING, THE DIMENSION OF DEVICE ALSO SHIRK.THE DEVICE CHANNEL LENGTH OF INTEGRATED CIRCUIT DOWN TO DEEP SUBMICRON 0.1 MM PROCES -S OR EVEN SMALLER. RELIABILITY ENGINEER ALWAYS PLAY A VERY IMPORTANT ROLE IN INTEGRATED C -IRCUIT.IN THE PAST TIME, THE PROBLEM OF LATCH UP ALWAYS CONFUSES THE WORKER WHO DEAL WITH INTEGRATED CIRCUIT.SO EVERYONE WANT TO PREVENT THE PROBLEM OCCURS.IT COULD BE CONTROL FROM THE LAYOUT OR THE PROCESS. UNFORTUNATE,IT DERIVERS THE AN OTHER SERIOUS PROBLEM-ESD AFTER THE LATCH UP IMMUNITY IS IMPROVED AND THE DERIVE DENSITY IS INCREASED.THESE CHANGING ALWAY -S TAKE EFFECT ON THE RELIABILITY OF INTEGRATED CIRCUIT. THERE ARE TWO PARTS INCLUDED IN THIS THESIS,ONE IS THAT WE USE TMAMEDICI TO FIND OUT THE BEST DESIGN RULE,AND WE ALSO ANALYSIS THE CURRENT FLOWLINE,THE DISTRIBUTION OF TEMPERATURE, LATCH UP IMMUNITY IN PROTECT DEVICE.THE OTHER WE ACHIEVE LVTSCR IN TSMC 0.35 MM PROCESS.WE ANALYSIS THE CHIPS AND TEST THE ABILITY OF ESD PROTECTION.ACCORDING TO THE RESULT,IT WILL OBTAIN HOW TO DESIGN TRIGGERING VOLTAGE,HOLDING VOLTAGE, AND THE HOLDING CURRENT THAT CAN REACH 100MA OR EVEN MORE.WE ALSO TEST THE DUAL-DIRECT HIGH CURRENT TRIGGERING ESD PROTECT CIRCUIT OF IC.THE LOWEST OF NEGATIVE AND POSITIVE ESD PROTECTION ABILITY CONFIRMS INDUSTRY STANDARD .

Keywords : ESD,LATCH UP,SCR

Table of Contents

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