Hazard Filtering Technique for Low-Power Circuit Design

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ABSTRACT

The close relationship between power consumption and heat dissipation makes low-power design techniques important knowledge for every CMOS designer. Of course, low-power circuit design is especially important in battery-operated systems like cellular telephones, personal digital assistants (PDA), wristwatches, hearing aids, pocket calculators, pagers and prospectively the handheld multi-media terminal. Battery-powered systems require consuming low power, so it is important to avoiding unnecessary activity to save the energy. This is the reason why we introduce the hazard elimination technique to achieve the low power consumption. Note that, eliminating hazard not only decreases the power consumption, but also reduces the function errors of circuits. The organization of this thesis is as follows. Chapter 1 introduces the low power developing condition and feature. Chapter 2 introduces the cause of the power consumption, and proceeds with the methods of reducing power consumption. Chapter 3 introduces three kinds of hazard (i.e., static-1 hazard, static-0 hazard, and dynamic hazard) and hazard filtering techniques. In chapter 4, we use a full adder as an example to illustrate our method, thinking about architecture, circuit design, flooring layout, and routing for the purpose of obtaining low-power and high-speed circuits. We simulate the circuits using Hspice simulator. The chip is fabricated in TSMC 0.35um technology. Finally, we make a conclusion in Chapter 5. Keywords: low power circuit design, hazard

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REFERENCES

[1]Luca Benini, Giovanni De Micheli, and Enrico Macii, “ Designing Low-Power Circuit: Practical Recipes, ” IEEE Circuits and ystems Magazine, Vol. 1, No. 1, PP. 6~25, 2001.

[2]Abdellatif Bellaouar and Mohamed I. Elmasry, “ Low-Power Digital VLSI Design Circuit and System ”, Toppan Kluwer, 1996.

[3]Sung-Mo Kang and Yusuf Leblebigi, “ CMOS Digital Integrated Circuits Analysis and Design ”, McGraw-Hill, 1999.

[4]H. J. M. Veendrick, “ Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on the Design of Buffer Circuits, ” IEEE J.

Solid-State Circuits, Vol. 19, No. 4, PP. 468~473, August 1984.
[5]S. M. Kang, “ Accurate Simulation of Power Dissipation in VLSI Circuits, ” IEEE J. Solid-State Circuits, Vol. 21, No. 5, PP. 889~891, October 1986.
[6]G. J. Fisher, “ An Enhanced Power Meter for SPICE2 Circuit Simulation, ” IEEE Trans. Computer-Aided Design, Vol. 7, PP. 641~643, May 1988.
[7]G. Y. Yacoub and W, H. Ku, “ An Enhanced Technique for Simulating Short-Circuit Power Dissipation, ” IEEE J. Solid-State Circuits, Vol. 24, No. 3, PP. 844~847, June 1989.
[8]S. Borkar, “ Design Challenges of Technology Scaling ” , IEEE Micro, Vol. 19, No. 4, PP. 23-29, July-August 1999.
[9]S. Thompson, P. Packan, and M. Bohr, “ Mos Scaling: Transistor Challenges for the 21st Century ” , Intel Technology Journal, Q3, 1998.
[10]S. Thompson, P. Packan, and M. Bohr, “ MOS Scaling: Transistor Challenges for the 21st Century ” , Intel Technology Journal, Q3, 1998.
[11]C. Piguet, J.-M. Masgonty, S. Cserveny, and E. Dijkstra, “ Low-Power Low-Voltage Digital CMOS Cell Design, ” in Proc. PATMOS ’ 94, Barcelona, Spain, PP. 132~139, October 1994.
[12]N. Ohkubo, “ A 4.4ns CMOS 54*54-b Multiplier using Pass-Transistor Multiplex, ” IEEE J. Solid-State Circuits, Vol. 30, PP. 251~257, March 1995.
[13]R. Zimmermann and W. Fichtner, “ Low-Power Logic Styles CMOS Versus Pass-Transistor Logic, ” IEEE J. Solid-State Circuits, Vol. 32, No. 7, PP. 1079~1090, July 1997.
[14]C. Piguet, J. M. Masgonty, P. Mosch, C. Arm, and V. von Kaenel, “ Low-Power Low-Voltage Standard Cell Libraries, ” in Proc. Low Voltage-Low Power Workshop, ESSCIRC ’ 95, Lille, France, Sept. 1995.
[15]R. Rogenmoser, H. Kaselin, and N. Felber, “ The Impact of Transistor Sizing on Power Efficiency in Submicron CMOS Circuits, ” in Proc. 22nd European Solid-State Circuit Conf., Neuchatel, Switzerland, Sept. 1996.
[16]Fu-Tsai Cheng, Tsung-Huan Chuang, and Jin-Hua Hong, “ Hazard Filtering Technique for the Prevention of Electric Magnetic Interference, ” 2001 Taiwan EMC Conference Broadband Narrowband EMI, PP.202~205, October 2001.
[17]Fu-Tsai Cheng, Yu-Jin Chen, Yi-Chi Yang, and Jin-Hua Hong, “ Hazard Filtering Technique for the Low-Power Wireless Communication, 2001 Cross Strait Wireless Communication Conference, N902038, December 2001.
[18]John F. Wakerly, “ Digital Design Principles and Practices, ” Combinational logic design principles, Vol. 3, No. 1, PP. 207~230, 1990.
[19]Dirk Rabe, Wolfgang Nebel, “ Short Circuit Power Consumption of Glitches, ” ISLPED Monterey CA USA, PP. 125~128, 1996.
[20]D. Rabe, “ New Approach in Gate-Level Glitch Modeling, “ EURO-DAC, 1996.
[21]Young-Hwan Yun, Ho-Jung Yoo, Seog-Heon Ham, Young-Jun Kim, and Yong-Hee Lee, “ A Filter for Low EMI and Low Noise, ” The First IEEE Asia Pacific Conference on 1999, PP. 17~20, 1999.
[22]T. Steinecke, “ Design-In for EMC on CMOS Large-Scale Integrated Circuits, ” 2001 EMC International Symposium on Electromagnetic Compatibility, Vol. 2, PP. 910~915, 2001.
[23]Masakazu Shoji, ” CMOS Digital Circuit Technology, ” Prentice Hall, Vol. 26, No. 5-6, PP. 403~407, 1988.
[24]S. Kim, J. Kim and S. Y. Hwang, “ New path balancing algorithm for glitch power reduction, ” IEE Proc-Circuits Devices System, Vol. 148, No. 3, PP. 151~156, June 2001.
[25]Sachio Hayashi and Masaaki Yamada , “ Noise Analysis Under ASIC Design Environment, ” IEEE Computer-Aided Design of Integrated Circuits and Systems, Vol. 19, No. 11 , PP. 1337~1346, November 2000.
[26]J. Gong and Eddie M. C. Wong, “ Verification of Asynchronous Circuits with Bounded Inertial Gate Delays, ” Test Symposium ATS '98. Proceedings, PP. 399~401, 1998.
[27]Vishwani D. Agrawal, “ Low-Power Design by Hazard Filtering, ” 10th International Conference on VLSI Design, PP. 193~197, January 1997.
[28]S. H. Unger, “ Asynchronous Sequential Switching Circuits, ” Wiley Inter-science, New York, 1969.
[29]Charles H. Roth, “ Fundamentals of Logic Design, ” West Publishing Company, Vol. 2, No. 1~6, PP. 653~675, 1992.
[30]Hasan Krad, “ Multilevel Combinational Circuits and Hazard Detection, ” Proc. IEEE Southeastcon, Vol. 1.2, PP. 573~575, 1992.
[31]Hanho Lee and Gerald E. Sobelman, “ A New Low-Voltage Full Adder Circuit, ” Proc. 7th Great Lakes Symposium on VLSI, PP. 88~92, 1997.
[32]Wayne Wolf, “ Modern VLSI Design Systems on Silicon, ” Prentice-Hall PTR, Vol. 3.4, PP. 138~141, 1998.