適用於低功率電路設計之突波濾波技術

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摘 要

功率消耗與散熱問題的緊密關係對於CMOS設計者而言，使得低功率技術成為一門重要的學問。當然低功率電路設計對於使用電池的系統像是衛星電話、個人數位秘書、手錶、助聽器、口袋式計算器、傳呼機及未來手持式多媒體終端機等，更是特別的重要。電池電源系統需要低功率消耗，所以要避免不必要的動作來節省電源是很重要的。本論文研究的動機即是以消除“突波”來達成降低功率消耗的目的，因為“消除突波”不僅可以降低功率的耗損，而且還可以減少電路工作的錯誤。 在本論文中，第一章介紹低功率發展現況與前景，第二章將功率消耗的成因、降低功率耗損的方法做詳細的介紹，第三章介紹突波的種類(如靜態1突波、靜態0突波及動態突波等)及突波濾波的技術，第四章採用上述的改良方法來設計全加器，在架構、電路設計、平面佈局及連線，我們均以低功率、高速度為設計重心，電路採用H-spice軟體模擬，並送交台積電(TSMC) 0.35μm製程技術製作晶片，以證明其可行性與可靠性，最後第五章做本論文之總結。 關鍵字：低功率電路設計、突波。

關鍵詞 : 低功率電路設計 ; 突波

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