

底電極薄膜電晶體研究與分析=research and analysis of undergate tft

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摘要

摘要 最近，複晶矽薄膜電晶體由於其廣泛應用在印表頭及成像器及平面顯示器上而受到廣泛的注意。傳統上，複晶矽薄膜電晶體有一層絕緣基板及大約12伏特的操作電壓，同時其電特性和複晶矽材料的特性也有極大的關聯。所以，我們不能以傳統上的MOSFET元件模式來描述複晶矽薄膜電晶體元件的操作。到目前為止，很少研究是針對複晶矽薄膜電晶體的元件模式，特別是已發展在MEDICI, TSUPREM4, 及AIM-SPICE電路模擬器上的I-V及C-V模式更是付之闕如。最近，部分應用在電路上的低溫複晶矽薄膜電晶體的論文已經發表，但是卻少有論文將溫度效應考慮在電路模式。尤其，更缺乏有關具有溫度效應的複晶矽薄膜電晶體模式建立到商用的電路模擬器上。本論文嘗試發展一套以物理基礎的複晶矽薄膜電晶體的I-V及C-V模式。首先，必須發展出一套複晶矽薄膜電晶體的元件模式以及其中參數的萃取方式，參數萃取主要由實驗資料而得，得到之後再帶回所發展德模式中驗證其正確性。所引用的數據主要為一下電極的TFT元件結構，閘極氧化層厚度為1000 \AA ，通道長度從1 μm 到6 μm ，且是低溫製程。經由上述步驟所得到的模式已放入SPICE電路模擬器中從而預測測及分析複晶矽薄膜電晶體的電路特性。在本論文中，我們將描述一個模式，此模式應用在次臨界到飽和區間都是可微分且連續，因此是一個非常適用於加入MEDICI, TSUPREM4, AIM-SPICE 電路模擬器。通道長度調變、速度飽和效應、Kink 效應、溫度效應、閘極偏壓誘使晶粒邊界位能降低(GIBL)、汲極偏壓誘使晶粒邊界位能降低(DIBL)、熱載子效應(Hot Carriers Effect)及溫度相依效應將被我們所探討與模式化。

關鍵詞：複晶矽薄膜電晶體；通道長度調變；Kink 效應；汲極偏壓誘使晶粒邊界位能降低

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參考文獻

Reference [1]張俊彥主編，鄭晃忠審校，「積體電路製程及設備技術手冊」；1998年經濟部技術處、中華民國產業科發展協進會、中華民國電子材料元件協會出版發行。

- [2]施敏原著，張俊彥譯著，「半導體元件物理及製作技術」；1996年，高立出版社出版。
- [3]陳連春編譯，「彩色液晶顯示器原理與技術」；建興出版社 [4]陳連春編譯，「最新彩色液晶技術」；建興出版社 [5]李雅明著，「固態電子學」；1984年，全華出版社 [6]莊人達編著，「VLSI製造技術」；1994年，高立圖書有限公司 [7]龍文安著，「積體電路微影製程」；1998年，高立圖書有限公司 [8]Michael Shur，" Introduction to Electronic Devices "；1995，John Wiley & Sons INC.
- [9]Teruhiko Yamazaki，Hideaki Kawakami，Hiroo Hori " Color TFT Liquid Crystal Display "；1995，SEMI Standard FPD Technology Group .
- [10]Toshihisa Tsukada，" TFT/LCD Liquid-Crystal Displays Addressed by Thin Film Transistors " Hitachi Ltd. Tokyo，Japan.
- [11]Vladimir G. Chigrinov " Liquid Crystal Devices : Physics and Applications " 1999 Artech House Boston London .
- [12]Tor A. Fjeldy，Trond Ytterdal，and Michael Shur " Introduction to Device Modeling and Circuit Simulation " 1998，John Wiley & Sons INC.
- [13]B. Streetman，Solid State Electronic Device，4th ed. Prentice-Hall，Englewood Cliffs，NJ (1993).
- [14]R.L Weisfield，H. C. Tuan，L. Fennell，and M. J. Thompson，" Amorphous Silicon Thin Films Transistors Array Technology :Application in Printing and Document Scanning "，Master. Res. Soc. Symp. Proc.，Vol.95, pp.469-474，1987 .
- [15]M.J Thompson and h. c. tuan，" amorphous silicon electronic devices and their applications "，in iedm tech. Dig.，pp192-195，Dec. 1986.
- [16]Hitoshi Aoki " Dynamic Characterization of a-Si TFT-LCD Pixels "，IEEE Transactions on Electron Device，VOL. 43, No.1, January 1996 .
- [17]R. A. Street，Hydrogenated Amorphous Silicon，Cambridge Solid State Science，1991 [18]T. Leroux，" Static and Dynamic Analysis of Amorphous Silicon Field-Effect Transistors " Solid-State Electron，Vol,29 ,No.1，pp.47-58，Jan.1986.
- [19]J. G. Shaw and M. Hack " An Analytic Model For Calculating Trapped Charge In Amorphous Silicon "，J. Appl. Phys., vol.64, No.9 pp. 4562-5466, Nov.1988 [20]K.Khakzar and E.H.Lueder，" Modeling of Amorphous-Silicon Thin-Film Transistors for Circuit Simulation with SPICE, " IEEE Trans. Electron [21]M. Shur and M. Hack，" Physics of Amorphous Silicon Based Alloy Field-Effect Transistors " J.Appl. Phys., vol. 55, no10, pp.3831-3842，1984 [22]M.J.Powell，" Charge trapping instabilities in amorphous silicon —silicon nitride thin film transistor，" Appl. Phys. Lett., vol 43, no. 6, pp. 597-599, 1983.
- [23]H.Aoki and E. Kigoshi，" A new semi-empirical model for amorphous silicon thin-film-transistors，" in Proc. 1993 Int. VPAD, pp. 138-139
- [24]N. Ibaraki, M. Kigoshi，K. Fukuda and J. Kobayashi，" Threshold voltage instability of a-Si:H TFT ' s in liquid crystal displays，" J. Non-Crystalline Solids，vol. 115, pp. 138-140, 1989.
- [25]A.Vladimirescu and S. Liu，" The simulation of MOS integrated circuits using SPICE2，" UCB/ERL M80/7，1980.
- [26]M. S. Shur, H. C. Slade, T. Ytterdal, L. Wang, Z. Xu, K. Afatoon, Y. Byun, Y. Chen, M. Froggatt, A. Krishnan, P. Mei, H. Meiling, B.-H. Min, A. Nathan, S. Sherman, M. Stewart, and S. Theiss, Modeling and Scaling of a-Si:H and Poly-Si Thin Film Transistors, Mat. Res. Soc. Symp. Proc., vol. 467, pp. 831-842 (1997) [27]M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, SPICE Models for Amorphous Silicon and Polysilicon Thin Film Transistors, J. Electrochem. Soc., Vol. 144, No. 8, pp. 2833-2839, (1997).
- [28]H.C. Slade and M. S. Shur, Analysis of Bias Stress on the Performance of Unpassivated Hydrogenated amorphous Silicon Thin Film Transistors, IEEE Trans. Electron Devices, accepted for publication.
- [29]M.S. Shur, H.C. Slade, T. Ytterdal, L. Wang, and Z. Xu, "Modeling and Scaling of a-Si:H and Polysilicon Thin Film Transistors," invited paper to be presented at the Materials Research Society Spring 1997 Meeting, Amorphous and Microcrystalline Silicon Technology, April 1997.
- [30]H. C. Slade, M. S. Shur, S. C. Deane, and M. Hack, "Below Threshold Conduction in a-Si:H TFTs With and Without a Silicon Nitride Passivating Layer," Applied Physics Letters, Vol. 69, No. 17, p. 2560 (October 1996).
- [31]A. Owusu, M. D. Jacunski, M. S. Shur, and T. Ytterdal, SPICE Model for the Kink Effect in Polysilicon TFTs, p. 680, in Meeting Abstracts, vol. 96-2, Fall Meeting, San Antonio, Texas, The Electrochemical Society, New Jersey, ISBN 0160-4619, October 6-11, 1996.
- [32]M. S. Shur, M. D. Jacunski, H. C. Slade, A. A. Owusu, T. Ytterdal, and M. Hack, SPICE Models for Amorphous Silicon and Polysilicon Thin Film Transistors, p. 559, in Meeting Abstracts, vol. 96-2, Fall Meeting, San Antonio, Texas, The Electrochemical Society, New Jersey, ISBN 0160-4619, October 6-11, 1996 [33]M.D. Jacunski, M.S. Shur, and M. Hack, "Threshold Voltage, Field Effect Mobility, and Gate to Channel Capacitance in Polysilicon TFTs," IEEE Trans. Elec. Dev., vol. 43, September 1996.
- [34]H.C. Slade, M.S. Shur, S.C. Deane, M. Hack, "Physics of Below Threshold Current Distribution in a-Si:H TFTs," Materials Research Society Proceedings, Amorphous Silicon Technology/Materials for Flat Panel Displays, vol. 420, p. 257 (April 1996).
- [35]M.D. Jacunski, M.S. Shur, T. Ytterdal, A.A. Owusu, and M. Hack, "AC and DC Characterization and SPICE Modeling of Short Channel Polysilicon TFTs," presented at the 1996 Materials Research Society Spring Meeting, San Francisco, CA, April 1996.
- [36]M. Shur, M. Jacunski, H. Slade, M. Hack, "Analytical Models for Amorphous and Polysilicon Thin Film Transistors for High Definition Display Technology," J. of the Society for Information Display, vol. 3, no. 4, p. 223, 1995.
- [37]H.C. Slade, "Material and Operational Characterization of Hydrogenated Amorphous Silicon Thin Film Transistors," The Electrochemical Society Interface, vol. 4, no. 4, p. 51, 1995.
- [38]M.D. Jacunski and M.S. Shur, "Drain Current and Capacitance Simulation of Polysilicon Thin Film Transistors," SEMICAD Device 2D Simulation Application Note, Dawn Technologies, Inc., 1995.

- [39]M. Jacunski, M. Shur, A. Owusu, T. Ytterdal, and M. Hack, "SPICE Models for N and P Channel Polysilicon Thin Film Transistors in All Regimes of Operation," in the AMLCDs 95 Workshop Proceedings, p. 134, September 1995.
- [40]H. Slade, M. Shur, and M. Hack, "Temperature Dependent Analytical Model of a-Si Thin Film Transistors," in Proceedings of the 1995 Material Research Society Spring Meeting, April 1995.
- [41]M. Jacunski, M. Shur, and M. Hack, "New Interpretation of Threshold Voltage in Polysilicon TFTs: A Theoretical and Experimental Study," in the Device Research Conference Digest, p. 158, June 1995.
- [42]M. Shur, M. Jacunski, and M. Hack, "Device and Circuit Models for Amorphous Silicon and Polysilicon Thin Film Transistors Used in High Definition Display Technology," in Proceedings of the IDRC, p. 45, 1994.
- [43]H. Slade, T. Globus, M. Shur, B. Gelmont, and M. Hack, "Effect of Stress on the Density of Deep Localized States in Amorphous Silicon Thin Film Transistors," in Electrochemical Society Fall Meeting Conference Proceedings, 1994.
- [44]T. Globus, H. Slade, M. Shur, and M. Hack, "Density of Deep Bandgap States in Amorphous Silicon from the Temperature Dependence of Thin Film Transistor Current," in Materials Research Society Symposium Proceedings, vol. 336, p. 823, 1994.