A Study of ESD Immunity Improvement for the Output Driver in Computer Fan ICs

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ABSTRACT

In this thesis, we take an output driver which can drive large current in computer fan ICs for HBM ESD stress. We also design protection circuits to improve ESD robustness by various layout parameters and structures. From the ESD testing result, it was found that the PS mode is weakest for the output driver of computer fan ICs during ESD stress. Eventually, the FOD＆SCR protection circuits were used to protect the whole-chip ESD stress, and put those circuits between the output pad vs. VDD pad and output pad vs. ground pad. Obviously, the ESD immunity in PS mode has been improved in an FOD protection circuit of output driver, the device with channel length L = 4um and with gate couple, and L = 2um with large parasitical base resister, were fabricated by the TSMC 0.6um process. In the same token, the ESD immunity level is also improved too, when an LVTSCR with drain-tap space equals to 4um.

Keywords : Output Buffer ; HBM ; ESD ; FOD ; SCR ; LVTSCR

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