RESEARCH AND DESIGN IN HARDWARE ARCHITECTURE OF DIGITAL BEAMFORMING RECEIVER

賴曉輝、黃其泮

E-mail: 9019011@mail.dyu.edu.tw

ABSTRACT

THE THESIS FOCUSES ON THE RESEARCH AND DESIGN OF DIGITAL BEAMFORMING RECEIVER'S HARDWARE ARCHITECTURE. THE RECEIVING FRONT-END CONSISTS OF AN ARRAY OF SENSORS (ANTENNAS) BY THE BEAMFORMING TECHNIQUES, WE CAN ARRIVE AT THE GOAL OF SPACE DIVISION MULTIPLE ACCESS IN WIRELESS ENVIRONMENT. THE ADAPTIVE PROCESSOR DETECTS THE DIRECTION OF ARRIVAL (DOA) OF EACH SOURCE SPREADING IN SPACE AND ESTIMATES THE OPTIMAL WEIGHT VECTOR. CONSEQUENTLY, ADAPTIVE BEAMFORMING CAN BE USED TO INCREASE SYSTEM CAPACITY. ONE OF THE MAIN ISSUES IN SPACE DIVISION MULTIPLE ACCESS (SDMA) IS A TECHNIQUE OF SMART ANTENNA. THE SMART ANTENNA CAN IMPROVE PERFORMANCE IN SEVERAL WAYS ：(1) TO INCREASE SPECTRAL EFFICIENCY AND SYSTEM CAPACITY.(2) TO REDUCE MULTI-PATH INTERFERENCE.(3) TO COMBAT CO-CHANNEL INTERFERENCE(CCI).(4) RANGE EXTENSION. IN THIS TEXT, WE APPLY THE BAND-PASS SAMPLING THEOREM FOR IF SAMPLING OF THE ARCHITECTURE OF SOFTWARE RADIO. FURTHERMORE, WE COMPLETED INTERFACE-CIRCUIT AND CONTROL-SOFTWARE WHICH CAN CONTROL MULTI-DIGITAL DOWN CONVERTER IN ONE COMPUTER SIMULTANEOUSLY, AND REALIZE THE DIGITAL BEAMFORMING(DBF) MODULE BY FIELD PROGRAMMABLE GATE ARRAY (FPGA). THE CONTROL-SOFTWARE OF VIEW INTERFACE SOFTWARE IS WRITTEN BY BORLAND C++ BUILDER (BCB) . IT CONTAINS THREE VIEW FORM ：(1) TO EXPLAIN ANY DIGITAL DOWN CONVERTER (DDC) MAGNITUDE INTERFACE (2) TO MONITOR EIGHTEEN DDC MAGNITUDE INTERFACE SIMULTANEOUSLY (3) TUNING INTERFACE. THE EIGHT-BITS ADJUST-ADDRESSER ON THE INTERFACE CIRCUIT CAN BE USED TOTAL TWO HUNDRED FIFTY-SIX ADDRESSES. THIS REACHES PURPOSE OF CONTROL MULTI-DDC. THE VERY HIGH DESCRIPTION LANGUAGE (VHDL) DESCRIBES DBF CIRCUIT TO ACCOMPLISH DBF BY XILINX 4036-3'S CHIP.

Keywords : BEAMFORMING, DIGITAL DOWN CONVERTER, BAND-PASS SAMPLING, DIGITAL RECEIVER

Table of Contents

REFERENCES

[1] 陳勝傑，軟體無線電架構下之數位升/降頻器設計與實現，元智大學電機工程研究所，碩士論文， 民八十九年六月。

[2] 施志偉，陣列天非線性訊號處理與DSP 實現，元智大學電機工程研究所，碩士論文，民九十年一 月。

[3] 張峰榆，多波束天線陣列設計與尋向定位應用，元智大學電機工程研究所，碩士論文，民八十九 年六月。

[4] 王國賢，智慧型天線於GSM 系統中基頻波束產生器之研製，元智大學電機工程研究所，碩士論文， 民八十八年六月。

[5] 胡元民，陣列天線通訊系統之移動通道模型與最佳化波束形成之研究，國立中興大學電機工程研 究所，碩士論文，民八十八年六月。

[6] 丁竑睿，軟體無線電架構下之GMSK 調變解調系統，元智大學電機工程研究所，碩士論文，民八十 八年六月。

[7] 邱志宇，軟體無線電架構性能分析，國立中興大學電機工程研究所，碩士論文，民八十九年六月。

[8] 劉仁俊、陳木松、黃其泮，遞迴式MVDR 於圓形陣列天線之信號低達角度偵測，兩岸三地研討會， 民八十八年。

[9] 陳世軒，適應性波束形成器之硬體設計與模擬，大葉大學電機工程研究所，碩士論文，民九十年 六月。

[10] 蒙以正，以MATLAB 透視DSP，基峰資訊，民八十八年十月。
[11] 曾振東、翁萬德、江松茶，通訊系統，全華科技，民八十七年十一月。-79- [12] 宗孔德、胡廣書，數位訊號處理，儒林，民八十五年六月。
[13] JOSEPH C. LIBERTI， JR.，SMART ANTENNAS FOR WIRELESS COMMUNICATIONS，PRENTICE HALLP -TR,1999.
[14] ANA PEREZ-NEIRA, XAVIER MESTRE, AND JAVIER RODRIGUES FONOLLOSA, UNIVERSITAT POLITECN -ICA DE CATALUNYA，SMART ANTENNAS IN SOFTWARE RADIO BASE STATION， IEEE COMMUNICAT -IONS MAGAZINE , VOLUME: 39 ISSUE: 2 , FEB. 2001 PAGE(S): 166 -173.
[15] N C DAVIES，A HIGH PERFORMANCE HF SOFTWARE RADIO，HF RADIO SYSTEMS AND TECHNIQUES, 2000. EIGHTH INTERNATIONAL CONFERENCE ON (IEE CONF. PUBL. NO. 474) , 2000 PAGE(S): 249 -256.
[16] MARK CUMMINGS, SHINICHIRO HARUYAMA，FPGA IN THE SOFTWARE RADIO，IEEE COMMUNICATIONS MAGAZINE , VOLUME: 37 ISSUE: 2 , FEB. 1999 PAGE(S): 108 -112.
[17] JOHN J. PATTI, ROBERT M. HUSNAY, AND JOSEPH PINTAR，A SMART SOFTWARE RADIO :CONCEPT DEVELOPMENT AND DEMONSTRATION， SELECTED AREAS IN COMMUNICATIONS, IEEE JOURNAL ON , VOLUME: 17 ISSUE: 4 , APRIL 1999 PAGE(S): 631 -649.
[18] ENRICO BURACCHINI，THE SOFTWATE RADIO CONCEPT，IEEE IEEE COMMUNICATIONS MAGAZINE , VOLUME: 38 ISSUE: 9 , SEPT. 2000 PAGE(S): 138 -143.
[19] JAVAD RAZAVILAR, FARROKH RASHID-FARROKHI , K. J. RAY LIU， SOFTWARE RADIO ARCHITECT -URE WITH SMART ANTENNAS :A TUTORIAL ON ALGORITHM AND COMPLEXITY，SELECTED AREAS IN COMMUNICATIONS, IEEE JOURNAL ON , VOLUME: 17 ISSUE: 4 , APRIL 1999 PAGE(S): 662-676.
[20] FAISAL SHAD, TERENCE D. TOLD, VYTAS KEZYS, AND JOHN LITVA，DYNAMIC SLOT ALLOCATION (DSA) IN INDOOR SDMA/TDMA USING A SMART ANTENNA BASESTATION，NETWORKING, IEEE/ACM TR -ANSACTIONS ON , VOLUME: 9 ISSUE: 1 , FEB. 2001 PAGE(S): 69 -81.
[21] OLLI VAINIO，DECIMATION AND INTERPOLATION OF NARROW-BAND SIGNALS，CONFERENCE OF THE IEEE , VO LUME: 3 , 1998 PAGE(S): 1362 -1365 VOL.3.
[22] OLLI VAINIO AND SAMI VALIVIITA，PREDICTIVE INTERPOLATION AND DECIMATION OF NARROW-BA -ND SIGNALS, INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON , VOLUME: 46 ISSUE: 5 , OCT . 1999 PAGE(S): 897 -903.
[23] R. PADKO, L. RIJNDERS, P. SCHAUMONT, S. VERNALDE AND D. DURACKOVA，HIGH-PERFORMANCE FLEXIBLE ALL-DIGITAL QUADRATURE UP AND DOWN CONVERTER CHIP，CUSTOM INTEGRATED CIRCU -ITS CONFERENCE, 2000. CICC. PROCEEDINGS OF THE IEEE 2000 , 2000 PAGE(S): 43 -46.
[24] SHAHRIAR EMAMI，NEW METHODS FOR COMPUTING INTERPOLATION AND DECIMATION USING POLYPH -ASE DECOMPOSITION，EDUCATION, IEEE TRANSACTIONS ON , VOLUME: 42 ISSUE: 4 [+CDROM] , NOV. 1999 PAGE(S): 311 -314.
[25] CHENG SHUIYING, CHEN PENGIV AND WU CHUANHUA，CONFIGURATION FOR THE TEN DIGITAL FILT -ERS OF HSP50214(A/B)，SIGNAL PROCESSING PROCEEDINGS, 2000. WCCC-ICSP 2000. 5TH INTE -RNATIONAL CONFERENCE ON , VOLUME: 1 , 2000 PAGE(S): 107 -117 VOL.1.
[26] RICHARD G. LYONS，UNDERSTANDING DIGITAL SIGNAL PROCESSING， ADDISON WESLEY,FEB 1999.
[27] PETER B. KENINGTON, LUC ASTIER，POWER CONSUMPTION OF A/D CONVERTERS FOR SOFTWARE RAD -IO APPLICATIONS，VEHICULAR TECHNOLOGY, IEEE TRANSACTIONS ON , VOLUME: 49 ISSUE: 2 , MARCH 2000 PAGE(S): 643 -650.