類比至數位轉換IC設計之研究

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摘 要

類比至數位轉換(ANALOG-TO-DIGTAL CONVERSION)是資訊或訊號處理過程中，不可或缺的一種介面技術。目前類比至數位轉換器中，並列比較方式(FLASH A/D)是屬於最高速的一種，轉換速度可高達奈秒(10-9SEC)，但這種方式的缺點是使用太多的比較器，晶片面積過大，成本較高。本論文希望提出一種兩階段並列放大比較式電路架構，可減少一半以上之比較器。最後並利用CMOS製程技術，設計製作出適當的運算放大器用於此A/D CONVERTER中。

關鍵詞 : 無

目錄

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