A STUDY OF ESD RELIABILITY ANALYSIS IN POWER MOSFET DEVICES

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ABSTRACT

THE ESD RELIABILITY IN POWER MOSFETS WILL BE INVESTIGATED IN THIS THESIS. THE TESTING SAMPLES WERE 100V LD NMOS, 200V LD NMOS, WHICH WERE DESIGNED AND DEVELOPED BY OURSELF, AND COMMERCIAL ICS WHICH WERE CONSISTED OF IRF640, RFW2N06RLE AND RLP03N06CLE. FROM THE EXPERIMENTAL RESULTS, ESD ZAP PULSES AT THE GATE TERMINAL WILL CAUSE ELECTRONS OR HOLES TRAPPED IN THE GATE OXIDE AND LOSSING THE SI-SIO2 INTERFACE INTEGRITY, ESPECIALLY FOR THE 100V LD NMOS, 200V LD NMOS, AND IRF640, IN WHICH THEY DO NOT HAVE ANY ESD PROTECTION CIRCUIT. ELECTRONS OR HOLES TRAPPING IN SIO2 LAYER WILL BE CAUSED THE THRESHOLD VOLTAGE INCREASING OR REDUCTION, AND EVEN RESULTED IN ELECTRON MOBILITY DEGRADATION. THE RFW2N06RLE AND RLP03N06CLE POWER VDMOS ICS WHICH WITH DIFFERENT KINDS OF ESD PROTECTION CIRCUIT ARE LESS INFLUENCED BY ESD PULSES EXPERIMENTALLY. MOREOVER, IN SOME SITUATION THE LATENT DAMAGE OF ELECTROSTATIC DISCHARGE IN A POWER MOSFET CAN'T EASILY FIND OUT IMMEDIATELY. EVENTUALLY, IN ORDER TO MAKE SURE A GOOD RELIABILITY AND LONG LIFETIME OF POWER MOSFETS, THE ESD PROTECTION CIRCUIT DESIGN TO PREVENT ESD DAMAGES IN A POWER MOSFET IS NECESSARY.

Keywords : 無

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