

高介電鈦酸鋇鋇薄膜電容元件之電漿蝕刻特性研究

廖芳慶、武東星

E-mail: 8919318@mail.dyu.edu.tw

摘要

鈦酸鋇鋇(BST)薄膜，因其獨特的電性與物理結構，目前應用極為廣泛，本論文主要探討其應用於動態隨機存取記憶體的電容特性，由於此材料目前在薄膜電容元件中，其漏電流將仍有待改善且縮小元件製程亦為目前積體化重要的關鍵技術之一，因此本論文將使用感應式耦合電漿 (ICP) 技術進行鈦酸鋇鋇表面處理來改善薄膜的電特性，並對其蝕刻機制與電漿導致的傷害進行研究。由於此研究關係到許多電漿基本特性的探討，所以本論文也以Langmuir探針電漿檢測系統對一些常用的電漿製程參數進行探討。於電漿處理部分，我們使用NH₃電漿針對鈦酸鋇鋇薄膜作處理，探討其在 Pt/BST/Pt電容結構的漏電流與電性，研究結果發現經過NH₃電漿處理的鈦酸鋇鋇薄膜在供應電壓1.5伏時，其漏電流可從10⁻⁷(A/cm²)下降至10⁻⁹(A/cm²)等級，這漏電流的改善，發現主要是由於氮原子的填入而減少薄膜氧空缺所貢獻的，經由X-ray 光電子頻譜儀 (XPS) 的量測證實，經電漿處理過的鈦酸鋇鋇薄膜將會有N 1s 的峰值出現，然而其薄膜的介電特性可能會因電漿導致的空間電荷或離子撞擊而降低介電常數，經由原子力電子顯微鏡的觀察，可發現經電漿處理過鈦酸鋇鋇薄膜表面型態將會改變，因此在電漿處理中，必須對漏電流與介電常數作一取捨。於蝕刻方面，我們使用Cl₂/CF₄、Cl₂/SF₆、Cl₂/Ar混合氣體針對腔體壓力、ICP功率、下電極射頻 (RF) 功率等參數進行探討，並使用熱化學平衡模擬軟體 (Thermo data) 針對氣體配方對BST的熱化學平衡反應進行模擬，進而提供蝕刻的研究參考。CF₄和SF₆兩種蝕刻氣體被發現會抑制蝕刻，猜測可能為沉積與蝕刻進行競賽的行為所致。在使用不同的Cl₂/Ar的混合氣體比時，化學輔助蝕刻的行為將被發現，且經由掃描式電子顯微鏡與原子力電子顯微鏡的觀察，發現在Ar/Cl₂的混合氣體下，加入30% Cl₂、ICP功率800 W、RF功率100 W 和腔體壓力5 mTorr時，將可得到一個平滑(粗糙度約1.8 nm)且沒有殘留物的表面。為了要更確定蝕刻的機制，我們使用X-ray光電子頻譜儀對鈦酸鋇鋇薄膜的表面反應特性進行研究，研究的結果發現，鋇原子將主要靠化學輔助物理(BaCl_x為可能產物)進行去除，對於去除鋇原子，物理性的撞擊將比化學性的氯蝕刻更有效率，而鈦則主要靠化學反應進行去除(TiCl_x為可能產物)，以上蝕刻的結果證實與化學熱平衡模擬計算的結果相符。然而在蝕刻時，可能會因一些電漿傷害而改變薄膜電容的特性，所以本論文以Pt/BST/Pt的電容結構針對漏電流與介電常數的變化探討其電漿導致傷害的機制，並對其電性恢復的方法進行研究。研究結果發現電漿會造成漏電流提高與介電損失，其中RF功率的提高可能為主要的影響因子。最後對於電漿傷害的元件，在經由氧氣600 °C的熱處理後發現其可有效率的恢復元件電性，其漏電流在1.5 V的偏壓下可小於3 × 10⁻⁷ (A/cm²)，而其相對二氧化矽的厚度約3.5 nm。

關鍵詞：鈦酸鋇鋇；高介電材料；薄膜電容；感應式耦合電漿；蝕刻；電漿導致傷害

目錄

1. Introduction	1
1.1 Application of BST in Gbit-Scale DRAM	1
1.2 Basic Properties of BST Films	3
1.3 Motivation of Plasma Treatment of BST Films	5
1.4 Motivation of BST Etching in an ICP System	6
2. Experiment Details	8
2.1 Preparation of BST Film	8
2.2 ICP System	11
2.3 Plasma Characteristics with Langmuir Probe	12
2.4 Plasma Treatment and Analysis of BST Films	13
2.5 Plasma Etching of BST Films	15
2.6 Damage Study of Pt/BST/Pt Capacitor	16
2.7 Measurements	17
3. Results and Discussion	17
3.1 Plasma Characteristics with Langmuir Probe	17
3.1.1 Plasma characteristics of Ar and Ar/Cl ₂ gas mixtures	20
3.1.2 Summary	25
3.2 Plasma Treatment of BST Films	26
3.2.1 Electrical properties	26
3.2.2 Physical properties	29
3.2.3 Mechanism of plasma treatment	30
3.2.4 Summary	32
3.3 Etching of BST Films	32
3.3.1 Basic mechanisms of etching	32
3.3.2 Simulation of thermo data	35
3.3.3 Etching effect of BST films	36
3.3.4 Etching mechanism of BST films	38
3.3.5 Summary	42
3.4 Damage Study of Pt/BST/Pt Capacitor	43
3.4.1 Overview of plasma-induced damage	43
3.4.2 Damage effects and recovery	44
3.4.3 Summary	47
4. Conclusions	48
References	51

參考文獻

References: [1] K. Kim, " Perspectives on giga-bit scaled DRAM technology generation ", Microelectronics Reliability, Vol. 40, p. 191-206, 2000.

- [2] T. Okuda, T. Murotani, "A Four-Level Storage 4-Gb DRAM", *IEEE J. Solid-State Circuits*, Vol. 32, p. 11, 1997.
- [3] K. P. Lee, Y. S. Park et al., "A Process Technology for 1Giga-Bit DRAM", *IEDM Tech. Dig.*, p. 907-910, 1995.
- [4] C. G. Hwang, S. I. Lee et al., "The state-of-the-art and future trend of DRAMs", *Microelectronic Journal*, Vol. 27, p. 777-783, 1996.
- [5] B. Gnade, S.R. Summerfelt et al., in: O. Auciello, R. Waser (Eds.), *Science, Technology of Electroceramic Thin Films: NATO ASI Series*, Vol. 284, Kluwer Academic Publishers, London, p. 373, 1995.
- [6] S. Ezhilvalavan, T. Y. Tseng, "Process in the developments of (Ba,Sr)TiO₃ (BST) thin films for Gigabit era DRAMs", *Materials Chemistry and Physics*, Vol. 65, p. 227-248, 2000.
- [7] Cheol Seong Hwang, "(Ba,Sr)TiO₃ thin films for ultra large scale dynamic random access memory. A review on the process integration", *Materials Science and Engineering*, Vol. 56, 178-190, 1998.
- [8] K. Ono, T. Horikawa et al., "(Ba,Sr)TiO₃ Capacitor Technology for Gbit-Scale DRAMs", *IEDM Tech. Dig.*, p. 803-806, 1998.
- [9] K. Hieda, K. Eguchi et al., "All Perovskite Capacitor (APEC) Technology for (Ba,Sr)TiO₃ Capacitor Scaling toward 0.1 μm Stacked DRAMs", *IEDM Tech. Dig.*, p. 807-810, 1998.
- [10] B. T. Lee, C. Y. Yoo et al., "Integration Process of (Ba,Sr)TiO₃ Capacitor for 1Gb and Beyond", *IEDM Tech. Dig.*, p. 815-817, 1998.
- [11] S. Yamamichi, P. Y. Lesaichere et al., "A Stacked Capacitor Technology with ECR Plasma MOCVD (Ba,Sr)TiO₃ and RuO₂/Ru/TiN/TiSix Storage Nodes for Gb-Scale DRAMs", *IEEE Trans. on electron devices*, Vol. 44, p. 7, 1997.
- [12] F. Tcheliobou, H. S. Ryu et al., "On the microstructure and optical properties of Ba_{0.5}Sr_{0.5}TiO₃ films", *Thin Solid Films*, Vol. 305, p. 30-34, 1997.
- [13] S. Yamaichi, A. Yamamichi et al., "Impact of Time Dependent Dielectric Breakdown and Stress-Induced Leakage Current on the Reliability of High Dielectric Constant (Ba, Sr)TiO₃ Thin-Film Capacitors for Gbit-Scale DRAMs", *IEEE Trans. on electron device*, Vol. 46, p. 342-347, 1999.
- [14] K. Eguchi, K. Hieda et al., "(Ba, Sr)TiO₃ Stacked Capacitor Technology for 0.13 μm-DRAMs and Beyond", *SSDM99, Tokyo*, p. 484-485, 1999.
- [15] M. S. Tasi, T. Y. Tseng et al., "Effect of Bottom electrodes on Resistance Degradation and Breakdown of (Ba, Sr)TiO₃ Thin Films", *IEEE Trans. on Components and Packaging Tech.*, Vol. 23, p. 128-135, 2000.
- [16] Y. Nishioka, K. Shiozawa et al., "Gib-bit Scale DRAM Cell with New Simple Ru/(Ba,Sr)TiO₃/Ru Stacked Capacitors Using X-Ray Lithography", *IEDM Tech. Dig.*, p. 903-906, 1995.
- [17] T. Iizuka, K. Arita et al., "Low Temperature Recovery of Ru/(Ba, Sr)TiO₃/Ru Capacitors Degraded by Forming Gas Annealing", *SSDM99, Toyko*, pp. 486-487, 1999.
- [18] Y. Tsunemine, T. Okudaira et al., "A manufacturable integration technology of sputter-BST capacitor with a newly proposed thick Pt electrode", *IEDM Tech. Dig.*, p. 811-814, 1998.
- [19] C. S. Kang, H. J. Cho et al., "Deposition Characteristics of (Ba, Sr)TiO₃ Thin Films by Liquid Source Metal-Organic Chemical Vapor Deposition at Low Substrate Temperatures", *Jpn. J. Appl. Phys.*, Vol. 36, p. 6946-6952, 1997.
- [20] A. Yuuki, M. Yamamuka et al., "Novel Stacked Capacitor Technology for 1 Gbit DRAMs with CVD-(Ba,Sr)TiO₃ Thin Films on a storage Node of Ru", *IEDM Tech. Dig.*, p. 115-122, 1995.
- [21] S. Yamamichi, P. Y. Lesaichere et al., "An ECR MOCVD (Ba,Sr)TiO₃ based stacked capacitor technology with RuO₂/Ru/TiN/TiSix storage nodes for Gbit-scale DRAMs", *IEDM Tech. Dig.*, p. 119-122, 1995.
- [22] H. Yamaguchi, T. Iizuka et al., "A stacked Capacitor with an MOCVD-(Ba,Sr)TiO₃ Film and a RuO₂/Ru Storage Node on a TiN-capped Plug for 4 Gbit DRAMs and beyond", *IEDM Tech. Dig.*, p. 675-678, 1996.
- [23] R. H. Horng, D. S. Wu et al., "Rapid-Thermal-Processed BaTiO₃ Thin Films Deposited by Liquid-Source Misted Chemical Deposition", *Jpn. J. Appl. Phys.* Vol. 37, p. 885-888, 1998.
- [24] K. S. Chang-Liao, J. M. Ku, "Improvement of oxynitride reliability by two-step N₂O nitridation", *Solid State Electronic*, Vol. 43, p. 2057-2060, 2000.
- [25] H. J. Cho, S. Oh et al., "Improvement of leakage current characteristics of Ba_{0.5}Sr_{0.5}TiO₃ films by N₂O plasma surface treatment", *Appl. Phys. Lett.*, Vol. 71, p. 3221-3223, 1997.
- [26] S. B. Kim, C. H. Kim et al., "Study on surface reaction of (Ba,Sr)TiO₃ thin films by high density plasma etching", *J. Vac. Sci. & Technol. A*, Vol. 17, p. 2156-2161, 1999.
- [27] H. M. Lee, D. C. Kim et al., "Inductively coupled plasma etching of (Ba,Sr)TiO₃ thin films", *J. Vac. Sci. Technol. B*, Vol. 16, p. 1891-1893, 1998.
- [28] S. P. DeOrnellas, A. Cofer, "Etching new IC materials for memory devices", *Solid State Technol.* Vol. 41, p. 53-58, 1998.
- [29] J. W. Lee, J. F. Donohue et al., "Mechanism of high density plasma processes for ion-driven etching of materials", *Solid-State Electronics*, Vol. 43, p. 1769-1775, 1999.
- [30] J. H. Joo, Y. C. Jeon et al., "Effects of Post-Annealing on the Conduction Properties of Pt/(Ba, Sr)TiO₃/Pt Capacitors for Dynamic Random Access Memory Applications", *Jpn. J. Appl. Phys.*, Vol. 36, p. 4382-4385, 1997.

- [31]K. R. Milkove, Integr. Ferroelectrics, Vol. 21, p. 53, 1998.
- [32]Handbook of X-ray Photoelectron Spectroscopy, J. Chastain (Perkin Elmer, Eden Prairie, MN, 1992), p. 44, 72, 105 ?.
- [33]Foundations of Materials Science and Engineering, 3nd, W. F. Smith (McGraw-Hill, New York, 1996), Ch. 2, p. 46.
- [34]K. R. Milkove, J. A. Coffin, " Effect of argon addition to a platinum dry etch process ", J. Vac. Sci. Technol. A, Vol. 16, p. 1483-1488, 1998.
- [35]D. Park, C. Hu, " The prospect of process-induced charging damage in future thin gate oxides ", Microelectronics Reliability, Vol. 39, p. 567-577, 1999.
- [36]C. R. Viswanathan, " Plasma-induced Damage ", Microelectronic Engineering, Vol. 49, p. 65-81, 1999.
- [37]E. van der Drift, R. Cheung et al., " Dry etching and induced damage ", Microelectronic Engineering, Vol. 32, p. 241-253, 1996.
- [38]Y. Fukuzumi, K. Natori et al., " Enhanced Recovery from Back-End Process Damage by Conductive Perovskite Electrode for BST Capacitor ", SSDM99, Tokyo, p. 488-489, 1999.
- [39]C. W. Chung, C. J. Kim, " Etching Effects on Ferroelectric Capacitors with Multilayered Electrodes ", Jpn. J. Appl. Phys., Vol. 36, p. 2747-2753, 1997.