A Study of ESD Protection Circuit Design in Power MOSFET ICs

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ABSTRACT

In recent years, power MOSFETs are widely used in many electric systems such as automatic electronics, power switching, power rectifier, and display driver. Two kinds of efficient ESD protection circuit design in lateral DEMOS(LDMOS) power transistor will be presented in this thesis. One kind of the test samples fabricated by our design was using gate-coupled technique, which was well designed the overlap between the drain and the gate for optimum the gate potential transient corresponding to maximum substrate current generated by ESD pulse, meanwhile, it can subsequently lead to forward biasing of the substrate-source junction and then turn on the parasitic bipolar transistor. Also, the other of the test samples were with an SCR structure, which is the most efficient of all protection devices in terms of ESD performance per unit area. Eventually, a SCR with polygate which will have a small trigger voltage under ESD event, and then it can obtain an efficient ESD protection.

Keywords : ESD ; POWERMOS ; LDMOS ; DEMOS

Table of Contents

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