功率mos元件esd保護電路設計之研究

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摘 要

近年來功率半導體元件被廣泛的應用於工業、商業、住家、通訊、交通與電力等領域。在未來的數十年內，電力電子將朝向高電壓、大電流功率、及低切換模組等方向發展，並且朝向積體電路化。然而，在此領域一直為人所遺忘的靜電放電破壞(ESD)問題卻依然存在，甚至比一般低電壓製程之積體電路更脆弱，本論文將針對時下最熱門的液晶顯示器驅動功率晶體(TFT LCD Driver IC)來設計其靜電放電保護電路，使其能符合業界靜電放電破壞之標準。 論文中將提出四種針對汲極延伸金氧半場效電晶體(DEMOSFET) 所設計之靜電保護電路，其一為採用CMOS製程之矽控閘流體(SCR)來保護DEMOSFET之汲-源極，靠靜電放電事件中之高電壓，使p-n-p-n接面產生崩潰而發生Latch up，形成一極低阻抗之電流消散路徑；其二為改良原矽控閘流體(SCR)，增加一複晶矽閘極(Poly Gate)與一高通RC濾波電路，以提升SCR之工作穩定性；其三為採用閘極耦合之方式，以汲極耦合至閘極之電位來誘發基板電流，使內部寄生之雙載子電晶體能在靜電放電事件中，提早被觸發導通，形成一低阻抗之靜電放電路徑。其四為結合一短通道閘極耦合金氧半場效電晶體(GCMOSFET)來保護DEMOSFET之閘極，利用第三項之原理並配合短通道元件導通快速之特性，針對閘極對高電壓與CDM (Charge Device Model) 高頻放電最敏感的弱點加以保護，再加以結合SCR或閘極耦合之方法來保護汲-源極，使DEMOSFET能獲得全方位之防護。

關鍵詞 : 靜電放電 ; 功率場效電晶體

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