

# Developing a Hardware Coprocessor for Petri-Net Execution

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## ABSTRACT

The ECAM is derived from CAM, which proposed a virtual word concept to construct an extensible architecture on a single chip. The virtual word has been proved that can effectively simplify the word length adjustment and reduce the overhead compared with the traditional CAM architecture. The ECAM also proposed FCMO that is one physical word of the virtual word that is designed to represent the concise information about the related virtual word. It is designed to provide another matched information to abound the applications of the matched virtual word. For example, ECAM is applied to identify the triggerable transition in a Petri net. The FCMO can directly represent an identified triggerable transition to simply the following processes of Petri net execution. Therefore, the ECAM is further applied to the design of Petri net execution coprocessor, which makes the triggerable transition identification and token updating in a constant time. So, the Petri net execution coprocessor based on the ECAM can promote the Petri net being applied to the applications of real time systems and control systems. Moreover, the prototyping and implementation of ECAM has adopted the FPGA, because the FPGA owns the capability of reconfigurable hardware. It is helpful on the design, implementation, performance evaluation, and function improvement of ECAM.

Keywords : Petri Net Model ; Extensible Content Addressing Memory ; Triggerable Transition

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## REFERENCES

1. J. L. Peterson, Petri Net Theory and Modeling of Systems, Prentice Hall, 1981.
2. J. M. Proth and X. Xie, Petri Net: A Tool for Design and Management of Manufacturing Systems, John Wiley & Sons, 1996.
3. N. Chang and W. H. Kwon, "FPGA-Based Implementation of Synchronous Petri Nets," IEEE IECON. 22nd International Conference on Industrial Electronics, Control, and Instrumentation, pp.469- 474, 1996.
4. C. P. Hwang and C. S. Ho, "Hardware Design of a Real-Time Petri Net Model for Real-Time Tasks," Journal of the Chinese Institute of Engineers, vol. 18, no. 4, pp. 481- 492, 1995.
5. N. Chang, J. Park, K. Koo, and W. H. Kwon, "Memory-Based Implementation of a Petri Net and its Application to a Programmable Controller," IEEE Proceedings of the IECON '93. International Conference on Industrial Electronics, Control, and Instrumentation, pp. 613-618, 1993.
6. R. P. Mayer, "A Variable Access Associative Memory Chip for Flexible Searches in RAM," Proceedings of the 1995 IEEE Fourteenth Annual International Phoenix Conference, pp. 102-108, 1995.
7. T. Ogura, J. Yamada, S. I. Yamada, and M. Tan-no, "A 20-kbit Associative Memory LSI for Artificial Intelligence Machines," IEEE Journal of Solid-State Circuit, vol. 24, no. 4, pp. 1014-1020, 1989.
8. Max, "Xilinx(pc) Training Course," Chip Implementation Center, Feb. 1999.
9. Xilinx, "XC4000E and XC4000X Series Field Programmable Gate Arrays," Version 1.5, 1999.
10. Tony, "Altera (pc) Training Course," Chip Implementation Center, Feb. 1999.
11. M. M. Mano, Computer System Architecture, 3rd ed., Prentice Hall, 1993.
12. T. Nikaido, T. Ogura, S. Hamaguchi, and S. Muramoto, "A 1-kbit Associative Memory LSI," Japan. J. Appl. Phys., vol. 22, pp. 51-54, 1983.
13. T. Higuchi, T. Furuya, K. Handa, and A. Kokubu, "IXM2:

A Parallel Associative Processor for Semantic Net Processing-Preliminary Evaluation, " Proceedings of the 2nd International IEEE Conference on Tools for Artificial Intelligence, pp. 667-673, 1990. 14. H. Tanaka, M. Hikichi, Y. Maruyama, Y. Cai, K Okuno, and T. Sekiguchi, " A Method for Adding Counter-Places to the Incidence Matrix of Petri Net, " IEEE Proceedings of the International Conference on Industrial Electronics, Control, Instrumentation, and Automation, pp.1422-1426, 1992. 15. T. L. Floyd, Digital Fundamentals, 5th ed., Prentice Hall, 1994. 16. 林傳生, 「使用VHDL電路設計語言之數位電路設計」, 儒林圖書, 1998。