以硬體方式輔助派翠網之執行作業=developing a hardware coprocessor for petri-net execution

李柏成、黃其泮

E-mail: 8804786@mail.dyu.edu.tw

摘 要

ECAM提出虛擬字組的概念，建立在同一硬體晶片中具內部擴接彈性的CAM結構，簡化字組寬度的調整；以及降低了傳統CAM在字組寬度擴展的字組虛耗。另一方面，ECAM提出FCMO的概念，以一實體字組用以代表存於ECAM中虛擬字組的精要含意，用以豐富地應用比對成功後的資訊表示型式，例如在派翠網的應用時，可將確任出可觸發轉換的代碼直接輸出，而不須經由比對結果來進一步判定可觸發轉換的傳統方式。 ECAM非常適合大資料寬度以及巨量資料搜尋，所以我們將它架構運用於派翠網執行協同處理器，以加速尋找可觸發之轉換，以ECAM為基礎的派翠網執行協同處理器將可彈性地適用不同大小的派翠網模型。此外，ECAM的硬體結構設計與實作以FPGA元件來完成，採用FPGA的研究目的是借用其可重組硬體的特性，進行各式ECAM構成模組的設計、實作、評量、與改善等研發歷程。

關鍵詞 : 派翠網模型 ; 可擴展的內容定址記憶體 ; 可觸發的轉換

目錄

參考文獻

1. J. L. Peterson, Petri Net Theory and Modeling of Systems, Prentice Hall, 1981. 2. J. M. Proth and X. Xie, Petri Net: A Tool for Design and Management of Manufacturing Systems, John Wiley & Sons, 1996. 3. N. Chang and W. H. Kwon, “ FPGA-Based Implementation of Synchronous Petri Nets, ” IEEE IECON. 22nd International Conference on Industrial Electronics, Control, and Instrumentation, pp.469- 474, 1996. 4. C. P. Hwang and C. S. Ho, “ Hardware Design of a Real-Time Petri Net Model for Real-Time Tasks, ” Journal of the Chinese Institute of Engineers, vol. 18, no. 4, pp. 481- 492, 1995. 5. N. Chang, J. Park, K. Koo, and W. H. Kwon, “ Memory-Based Implementation of a Petri Net and its Application to a Programmable Controller, ” IEEE Proceedings of the IECON ''93. International Conference on Industrial Electronics, Control, and Instrumentation, pp. 613-618, 1993. 6. R. P. Mayer, “ A Variable Access Associative Memory Chip for Flexible Searches in RAM, ” Proceedings of the 1995 IEEE Fourteenth Annual International Phoenix Conference, pp. 102-108, 1995. 7. T. Ogura, J. Yamada, S. I. Yamada, and M. Tan-no, “ A 20-kbit Associative Memory LSI for Artificial Intelligence Machines, ” IEEE Journal of Solid-State Circuit, vol. 24, no. 4, pp. 1014-1020, 1989. 8. Max, “ Xilinx(pc) Training Course, ” Chip Implementation Center, Feb. 1999. 9. Xilinx, “ XC4000E and XC4000X Series Field Programmable Gate Arrays, ” Version 1.5, 1999. 10. Tony, “ Altera (pc) Training Course, ” Chip Implementation Center, Feb. 1999. 11. M. M. Mano, Computer System Architecture, 3rd ed., Prentice Hall, 1993. 12. T. Nikaido, T. Ogura, S. Hamaguchi, and S. Muramoto, “ A 1-kbit Associative Memory LSI, ” Japan. J. Appl. Phys., vol. 22, pp. 51-54, 1983. 13. T. Higuchi, T. Furuya, K. Handa, and A. Kokubu, “ IXM2: A Parallel Associative Processor for Semantic Net Processing-Preliminary Evaluation, ” Proceedings of the 2nd International IEEE Conference on Tools for Artificial Intelligence, pp. 667-673, 1990. 14. H. Tanaka, M. Hikichi, Y. Maruyama, Y. Cai, K Okuno, and T. Sekiguchi, “ A Method for Adding Counter-Places to the Incidence Matrix of Petri Net, ” IEEE Proceedings of the International Conference on Industrial Electronics,

Control, Instrumentation, and Automation, pp.1422-1426, 1992. 15. T. L. Floyd, Digital Fundamentals, 5th ed., Prentice Hall, 1994. 16. 林傳生,「使用VHDL電路設計語言之數位電路設計」，儒林圖書，1998。