A Study of the Device Design in the Flash Memory

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ABSTRACT

The influence of bias conditions for program,erase operation and reliability for the flash memory device will be developed in ourstudy. The flash memory cell structure is a simple self-aligned doublepolysilicon with the stacked gate structure without any select transistor and a ONO layer were fabricated between the poly gates. Three kinds of device reliability contraints are examined for hot electrondegradation, hot electron avalanche breakdown, and time-dependent dielectric breakdown. Also, we will draw out an optimum design region of oxide thickness and channel length when the drain bias is 5V. Meanwhile, in our work, we will study the influences of program and erase operation under various bias situations, in which the operations are the channel hot electron injection,the source-side Fowler-Nordhiem erasing, the channel Fowler-Nordheim program and erasing, and the negative gate erasing. Eventually, we will hope that ourstudy in this work may be helpful in the next generation design.

Keywords : 快閃記憶體 ; 快閃記憶體元件設計

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