An Integer Linear Programming Approach to Large Scale 3D VLSI Incremental Floorplanning

梁峰碩、程仲勝

E-mail: 374893@mail.dyu.edu.tw

ABSTRACT

As the circuit modules need small changes of their locations and functions in a floorplan, incremental floorplanning is proposed to improve the floorplan quickly. In this thesis, Mathematical programming approach is used to solve the incremental floorplanning problem for large scale VLSI circuits to achieve layout optimization and shorten floorplanning time. It has better performance in solving incremental floorplanning for small scale VLSI circuits by using integer linear programming(ILP), however, as circuit function growing, chip area becomes larger, it is time-consuming for solving large scale VLSI incremental floorplanning problem by using ILP approach directly due to lots of constraints and variables. Therefore, the divide and conquer strategy is proposed to divide a VLSI circuit into some subcircuits, and the incremental floorplanning problem of each subcircuit is then solved by ILP efficiently. After each subproblem is conquered, merging procedures are applied to complete the whole incremental floorplanning problem.

Keywords : 3D IC、Incremental floorplanning、Integer linear programming

Table of Contents

REFERENCES

[1]W. Zhong, S. Chen and T. Yoshimura, “ Whitespace Insertion for Through-Silicon Via Planning on 3-D SoCs, ” IEEE Transactions on Circuit and System, pp. 913-916, May 2010.

[2]3D IC stacking technology Mar. 2010. http://www.2cm.com.tw/coverstory_content.asp?sn=1002260022.

[3]郭子熒，3D IC技術簡介與其發展現況，先進微系統與構裝技術聯盟季刊，第三十期，78~85頁，2008年。

[4]游淑惠，台灣半導體發展新紀元 – 3D IC，系統晶片第9期，3~10頁，2008年。

[5]A. Yoshida, J. Taniguchi, K. Murata, M. Kada, Y. Yamamoto, Y. Takagi, T. Notomi, A. Fujita, “ A Study on Package Stacking Process for Package-on-Package(POP) ”, Amkor Technology, Japan.

[6]D. H. Kim, S. Mukhopadhyay, and S. K. Lim, “ Through-Silicon-Via Aware Interconnect Prediction and Optimization for 3D Stacked ICs ”, SLIP, San Francisco, California, USA, July, 2009.

[7]D. M. Jang, C. Ryul, K. Y. Lee, B. H. Cho, J. Kiml, T. S. Oh, W. J. Lee and J. Yu, “ Development and Evaluation of 3-D SiP with Vertically Interconnected Through Silicon Vias (TSV) ”, Electronic Components and Technology Conference, 2007.

[8]M. Kawano, S. Uchiyama, Y. Egawa, N. Takahashi, Y. Kurita, K. Soejima, M. Komuro, S. Matsui, K. Shibata, J. Yamada, M. Ishino, H. Ikeda, Y. Saeki, O. Kato, H. Kikuchi and T. Mitsuhashi, “ A 3D Packaging Technology for 4 Gbit Stacked DRAM with 3 Gbps Data Transfer ”, IEDM, Shimokuzawa, Sagamihara, Kanagawa, Japan, 2006.

[9]P. D. Franzon, W. R. Davis, M. B. Steer, S. Lipa, E. C. Oh, T. Thorolfsson, S. Melamed, S. Luniya, T. Doxsee, S. Berkeley, B. Shani and K. Obermiller, “ Design and CAD for 3D Integrated Circuits ”, DAC, Anaheim, California, USA, June 2008.

[10]I. Loi, S. Mitra, T. H. Lee, S. Fujita and Luca Benini, “ A Low-overhead Fault Tolerance Scheme for TSV-based 3D Network on Chip Links ”, ICCAD, Toshiba, San Jose, CA, USA, 2008.

[11]Amkor Technology: http://www.amkor.com/.

[12]D. H. Kim, K. Athikulwongse, and S. K. Lim, “ A Study of Through-Silicon-Via Impact on the 3D Stacked IC Layout ”, ICCAD ’09, San Jose, California, USA, November 2-5 2009.

[13]J. Cong and M. Sarrafzadeh “ Incremental Physical Design ” Proceedings of International Symposium on Physical Design. 2000.

[14]Y. Liu, H. Yang and R. Luo“ An Incremental Floorplanner Based on Genetic Algorithm ” Proceedings of 5th International Conference on ASCI Vol.1, 2003, Pages 331-334.
[15]L. Yang, Y. Ma, X. Hong, S. Dong and Q. Zhou“ An Incremental Algorithm for Non-Slicing Floorplan Based on Corner Block List Representation ” Chinese Journal of Semiconductors Vol.26 No.12, 2005, Pages 2335-2343.
[16]高一宏、程仲勝，“ 植基於Corner Block List表示法之增量式平面規劃之研究 ”私立大葉大學電機工程研究所，2007年。
[17]Qing. Dong, Bo. Yang, Jing. Li,“ Incremental Buffer Insertion and Module Resizing Algorithm Using Geometric Progra μ ming ” Great Lakes Symposium on VLSI, 2009, Pages 413-416.
[18]張家銘、程仲勝，“ 植基於Corner Stitching表示法之增量式平面規劃之研究 ”私立大葉大學電機工程研究所，2007年。
[19]鄭威佑、程仲勝，“ 以整數線性規劃法解決3D超大型積體電路增量式平面規劃 ”私立大葉大學資訊工程研究所，2012年。