An Integer Linear Programming Approach to Large Scale Full-Custom VLSI Incremental Floorplanning

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ABSTRACT

In VLSI physical design phase, incremental floorplanning plays an important role. As the circuit modules need small changes of their structure in a floorplan, incremental floorplanning can be used to obtain a new floorplan solution quickly. Mathematical programming approach is one of effective methods which used to solve the incremental floorplanning problem. However, for large scale VLSI circuits, mathematical programming approach has aggravated efficiency problem due to a lot of constraints and variables. In this thesis, an integer linear programming approach is proposed for solving large scale VLSI incremental programming problem. In the proposed approach, divide and conquer strategy is first applied to cut the original floorplan block into small scale subblocks, and then a corresponding binary tree is created for each subblock to record topological relationships and whitespace sizes among modules by using corner stitching representation. Finally, the incremental floorplanning problem of each subblock is solved by integer linear programming approach without changing topological relationships and increasing subblock area. Experimental results show that the proposed incremental floorplanning strategy and algorithm can effectively modify module dimensions and shorten some connections for large scale 3D VLSI test circuits in an efficient way.

Keywords : Floorplanning、Incremental floorplanning、Mathematical programming

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