# A Novel Class - D Amplifiers Chip Design

## 陳瑞昌、李世鴻

E-mail: 374718@mail.dyu.edu.tw

#### ABSTRACT

This paper presents the design and implementation of a novel Class-D amplifiers chip. With low-power, high-performance, small area, and high speed, these circuits are employed in portable computer systems, such as the power circuits, electronic circuits, video and music amplifiers circuits, communications and control circuits, wireless communication and high-frequency circuit systems. This Class-D chip followed the chip implementation center advanced design flow, and then was fabricated using Taiwan Semiconductor Manufacturing Company 0.35-  $\mu$  m 2P4M mixed-signal CMOS process. The chip supply voltage is 3.3 V which can operate at a maximum frequency of 100 MHz. The total power consumption is 2.8307 mW, and the chip area size is 1.016 mm × 1.016 mm. Finally, the Class-D chip was tested and the experimental results are discussed. From the excellent performance of the chip verified that it can be applied to audio amplifiers, communications control, etc.

Keywords : Class-D, audio amplifier, pulse width modulation, control system

### Table of Contents

封面內頁 簽名頁 中文摘要	iii 英文摘要
iv 誌謝	∨目錄
vi 圖目錄	viii 表目錄
xiv 符號說明	xv 第一章 緒論 1.1 研究發展背景
11.2 研究動機	31.3 文獻回顧
4 1.4 設計流程	91.5 晶片設計流程圖
11 第二章 調變系統的設計與佈局 2.1 調	邊系統的原理與方法 12 2.2 脈波寬
度調變(PWM)控制IC系統架13 2.3 脈波罩	電度調變系統晶片實作成果
調變控制IC的切換方式 36 2.5 脈波寬	度調變控制IC時序分析
驗證部份 39 2.7 實作佈局專	☆證 44 2.8 PWM控制ⅠC
之規格列表 47 2.9 實測結果.	49 第三章 D類放大
器的電路分析與設計 3.1 傳統型理想半橋D類放大輸出電路	(P-ON)52 3.2 傳統型理想半橋D類放大輸出
電路(N-ON)55 3.3 傳統型實際半橋D类	頁放大電路(P-ON)57 3.4 傳統型理想
全橋D類放大電路 58 3.5 傳統型實	【際全橋D類放大電路60 3.6 新式平衡
式全橋D類放大電路62 3.7 新式實	【際平衡式全橋D類放大電路67 第四章 調
變系統的設計與佈局 4.1 新型平衡式全橋D類放大器	
波器	
波器 82 4.3 設計模擬的五種型態 	84 4.4 MOS電晶體模擬的12個區域 
波器	
波器82 4.3 設計模擬的五種型態 	
波器	
<ul> <li>波器</li></ul>	

圖 30 圖2.23 遲滯比較器訊	l號比較圖
遲滯曲線圖 31 圖2.25 雜訊對-	·般比較器的影響分析圖
號受雜訊影響分析圖	抗雜訊能力遲滯比較器訊號輸出圖
帶比較器電路輸入及輸出波形圖	遲滯比較器電路佈局圖
圖2.30 脈波寬度調變控制IC系統電路圖	圖2.31 脈波寬度調變控制IC系統電路佈局圖
圖2.32 電壓斜波電路輸出三角的波形圖	36 圖2.33 運算放大器電路輸出訊號的波形圖
	37 圖2.37 脈波實度調變控制IC時序分析圖
38 圖2 38 溫度對脈波實度調變系統的影響關係圖	39 圖2 39 雷厭轉換曲線對應不同 n/ n比值的變化特
性圖 40 圖2 40 PW/M 操作在50KHz時分析模擬圖	40 圖2 41 PWM操作在100KHz時分析模擬圖
41 图2 42 PW/M操作在200KHz时分析模擬图	42 圖2 43 PW/M操作在500KHz時分析模擬
圖 42 圖2 44 PW/M操作在1MHz時分析構構	
回	[圖
111回	J歌盘凰
一 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	G貝脰田力圖
期田計號(V-))ふく計號()	至生
「電路輸出訊號(Vout)端之訊號圖51 圖2.54 PVVN	晶方電路輸出訊號(Vout) 端之訊號圖
型理想半橋D類放大電路圖	
統型實際半橋D類放大電路圖	專統型埋想全稿D類放大電路圖
傳統型實際全橋D類放大電路圖60 圖3.0	5 創新的理想平衡式全橋D類放大電路圖
系統穩定度複數平面分析圖65 圖3.	8 新式實際平衡式全橋D類放大電路圖67
圖3.9 當SNR=5dB時, PWM訊號輸出波形圖69	9 圖3.10 當SNR=5dB時,Class D訊號輸出波形圖
69 圖3.11 當SNR=10dB時,PWM訊號輸出波形圖	. 70 圖3.12 當SNR=10dB時,Class D訊號輸出波形圖
70 圖3.13 當SNR=20dB時,PWM訊號輸出波形圖	. 71 圖3.14 當SNR=20dB時,Class D訊號輸出波形圖
71 圖3.15 當SNR=30dB時,PWM訊號輸出波形圖	. 72 圖3.16 當SNR=30dB時,Class D訊號輸出波形圖
72 圖3.17 當SNR=40dB時,PWM訊號輸出波形圖	. 73 圖3.18 當SNR=40dB時,Class D訊號輸出波形圖
73 圖3.19 當SNR=50dB時,PWM訊號輸出波形圖	. 74 圖3.20 當SNR=50dB時,Class D訊號輸出波形圖
74 圖3.21 當SNR=60dB時,PWM訊號輸出波形圖	. 75 圖3.22 當SNR=60dB時,Class D訊號輸出波形圖
75 圖3.23 當SNR=70dB時,PWM訊號輸出波形圖	. 76 圖3.24 當SNR=70dB時,Class D訊號輸出波形圖
76 圖3.25 當SNR=80dB時,PWM訊號輸出波形圖	. 77 圖3.26 當SNR=80dB時,Class D訊號輸出波形圖
77 圖4.1 新式平衡式全橋D類放大電器路圖	. 80 圖4.2 新型D類放大器輸出級和LC低通濾波器電路圖
82 圖4.3 新型D類放大器輸出級電路佈局圖	
84 圖4.5 新型D類放大器系統晶片佈局平面圖	. 87 圖4.6 新型D類放大器實體晶片光學微影圖
87 圖4.7 運算放大器輸入訊號(Vin-)端之量測圖	88 圖4.8 運算運算放大器輸出訊號(V-)端之量測圖
88 圖4 9 運算放大器輸出訊號與三角斜波訊號量測圖	89 圖4 10 雷厭斜波產生器輸出(2MHz)三角波訊號圖
90 周4 11 雷厭斜波產生哭輸出(5MHz)三角波訊號圖	
	01 圖4.14 雷厭到波產生哭齡出(100MHz)三角波訊號
回	
分析圖 101 圖4.27 當SNR=10dB時, 聲頻訊號300Hz的頻	1. 101 圖4.28 當SNR=20dB時, 登頻訊號300Hz的頻
譜分析圖 102 圖4.29 富SNR=30dB時,聲頻訊號300Hz的頻	龍分析圖… 102 圖4.30 富SNR=40dB時,      登損計號300Hz的損     ジェニュー     ジェニュー
譜分析圖 103 圖4.31 富SNR=50dB時,聲頻訊號300Hz的頻	龍行
: 語分析圖 104 圖4.33 當SNR=70dB時, 聲頻訊號300Hz的頻	龍晉分析圖… 104 圖4.34 當SNR=80dB時,聲頻訊號300Hz的頻
譜分析圖 105 圖4.35 當SNR=90dB時,聲頻訊號300Hz的頻	籍治析圖 105 表目錄 表1. PWM控制IC之功率消耗說明
表 85 表8. 新型D類放大器系統晶片規格表	85 符號說明 R:電阻(單位:歐姆 )。 L:電感(單位
:亨利H)。 C:電容(單位:法拉F)。 V:電壓(單位:伏特V)	。 I:電流(單位:安培A)。 P:功率(單位:瓦特W)。 L:長

度(單位:微米μm)。 W:寬度(單位:微米μm)。 Vt:臨界電壓或切入電壓(單位:伏特V)。 Vgs:閘-源電壓(Vgs =Vgate-Vsource)。 Vds:汲-源電壓(Vds =Vdrain- Vsource)。 ID:汲極電流。 f :頻率(單位:赫茲Hz)。 :角頻率( =2 f )。 Av :電壓增益。 PM:相位角。 GB:增益頻寬。

#### REFERENCES

[1]S. Nonaka and Y. Neba, "Single Phase PWM Current Source Converter with Double-Frequency Parallel Resonance Circuit for DC Smoothing," IEEE Industry Applications Society Annual Meeting, pp. 1144 – 1151, 1993.

[2]S. El-Hamamsy, "Design of High-Efficiency RF Class D Power Amplifier," IEEE Transactions on Power Electronics, Vol. 9, pp. 297 – 308, May 1994.

[3] Jong-Lick Lin, Hsin-Ying Hsieh, "Dynamics Analysis and Controller Synthesis for Zero-Voltage-Transition PWM Power Converters," IEEE Transactions on Power Electronics, Vol. 15, No. 2, pp. 205 – 214, March 2000.

[4]Dong-Yun Lee, Byoung-Kuk Lee, Sang-Bong Yoo, and Dong-Seok Hyun, "An Improved Full-Bridge Zero-Voltage-Transition PWM DC/DC Converter with Zero-Voltage/ Zero-Current Switching of the Auxiliary Switches, " IEEE Transactions on Industry Applications, Vol. 36, No. 2, pp. 558 – 566, April 2000.

[5] Joseph S. Chang, Meng-Tong Tan, Zhihong Cheng, and Yit-Chow Tong, "Analysis and Design of Power Efficient Class D Amplifier Output Stages, "IEEE Transactions on Circuits and Systems I, Vol. 47, No. 6, pp. 897 – 902, June 2000.

[6]W. C. Lo, C. C. Chan, Z. Q. Zhu, Lie Xu, and K. T. Chau, "Acoustic Noise Radiated by PWM-Controlled Induction Machine Drives," IEEE Transactions on Industrial Electronics, Vol. 47, No. 4, pp. 880 – 889, August 2000.

[7]Bah-Hwee Gwee, Joseph S. Chang, and Huiyun Li, "A Micro Power Low-Distortion Digital Pulse width Modulator for a Digital Class D Amplifier," IEEE IEEE Transactions on Circuits and Systems II, Vol. 49, No. 4, pp. 245 – 256, April 2002.

[8]S. Nonaka, "A Utility-Connected Residential PV System Aapted a Novel Single-Phase Composit PWM Voltage Source Inverter," IEEE Photovoltaic Specialists Conference, pp. 1064 – 1068, 1994.

[9]S. Nonaka and Y. Neba, "Single Phase Composit PWM Voltage Source Converter," IEEE IAS, pp. 761 – 767, 1994.

[10] Louis R. Nerone, "A Mathematical Model of the Class D Converter for Compact Fluorescent Ballasts," IEEE Transactions on Power Electronics, Vol. 10, No. 6, pp. 708 – 715, November 1995.

[11] I. D. Mosely et al., "Effect of Dead Time on Harmonic Distortion in Class-D Audio Amplifiers," Electronics Letters, Vol. 35, No. 12, pp. 950 – 952, June 1999.

[12] A. Hajimiri, and S. Limotyrakis, "Jitter and Phase Noise in Ring Oscillators," IEEE Journal of Solid – State Circuits, Vol. 36, No. 6, pp. 790 – 804, 1999.

[13] Meng Tong Tan, Joseph S. Chang, Hock Chuan Chua, and Bah Hwee Gwee, "An Investigation Into the Parameters Affecting Total Harmonic Distortion in Low-Voltage Low-Power Class-D Amplifiers," IEEE Transactions on Circuits and Systems I, Vol. 50, No. 10, pp. 1304 – 1315. October 2003.

[14] Marco Berkhout, "An Integrated 200-W Class-D Audio Amplifier," IEEE Journal of Solid-State Circuits, Vol. 38, No. 7, pp. 1198 – 1206, July 2003.

[15]B.J. Patella, A. Prodic, D. Maksimovic, "High-Frequency Digital PWM Controller IC for DC – DC Converters," IEEE Transactions on Power Electronics, Vol. 18, No. 1, pp. 438 – 446, January 2003.

[16] Cheung Fai Lee and Philip K. T. Mok, "A Monolithic Current-Mode CMOS DC – DC Converter With On-Chip Current-Sensing Technique," IEEE Journal of Solid-State Circuits, Vol. 39, No. 1, pp. 3 – 14, January 2004.

[17]J. Mahattanakul, "Design Procedure for Two-Stage CMOS Operational Amplifiers Employing Current Buffer," IEEE Transactions on Circuits and Systems II, Vol. 52, No. 11, pp. 766 – 770, 2005.

[18] Girish. Kurkure, Aloke K. Dutta, "A Novel Adaptive Biasing Scheme for CMOS Op-Amps," Journal of Semiconductor Technology and Science, Vol. 5, No. 3, pp. 168 – 172, 2005.

[19]J. K. Fiorenza, T. Sepke, and P. Holloway, "Comparator-Based Switched-Capacitor Circuits for Scaled CMOS Technologies," IEEE Journal of Solid – State Circuits, Vol. 41, No. 12, pp. 2658 – 2668, 2006.

[20]B. Goll, H. Zimmermann, "A Comparator with Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V," IEEE Transactions on Circuits and Systems II, Vol.56, No.11, pp. 810-814, 2009.

[21] M. A. Rojas-Gonzalez, E. Sanchez-Sinencio, "Low-Power High-Efficiency Class D Audio Power Amplifiers," IEEE Journal of Solid-State Circuits, Vol. 44, No. 12, pp. 3272 – 3284, 2009.

[22]A. M. Hava, E. Un, "A High-Performance PWM Algorithm for Common-Mode Voltage Reduction in Three-Phase Voltage Source Inverters," IEEE Transactions on Power Electronics, Vol. 26, No. 7, pp. 1998 – 2008, 2010.

[23] M. Berkhout, L. Dooper, "Class-D Audio Amplifiers in Mobile Applications," IEEE Transactions on Circuits and Systems I, Vol. 57, No. 5, pp. 992 – 1001, 2010.

[24]B. Leung, "A Switching-Based Phase Noise Model for CMOS Ring Oscillators Based on Multiple Thresholds Crossing," IEEE Transactions on Circuits and Systems I, Vol. 57, No.11, pp. 2858 – 2869, 2010.

[25] Ming Li, R. E. Amaya, "Design of mM-W Fully Integrated CMOS Standing-Wave VCOs Using Low-Loss CPW Resonators," IEEE Transactions on Circuits and Systems II, Vol. 59, No. 2, pp. 78 – 82, 2012.

[26] Ruei-Chang Chen, Yeong-Chau Kuo and Shih-Fong Lee, "High-Performance Pulse Width Modulation Chip Design for Mixed-Signal Integrated Circuits," National Conference on Modern Electrical Engineering Technologies, Vol. 1, pp. 172 – 177, 2006.

[27] Ruei-Chang Chen and Shih-Fong Lee, "Design and Layout of a High-Performance PWM Control Class D Amplifiers IC Systems," Applied Mechanics and Materials, Vol. 203, pp. 469 – 473, August 2012.

[28] Ruei-Chang Chen, Shih-Fong Lee and Yeong-Chau Kuo, " Low Power Pulse Width Modulation Design for Class D Audio Amplifier Systems, " Lecture Notes in Computer Science, Vol. 7473, pp. 136 – 143, August 2012.