An Integer Linear Programming Approach to 3D VLSI Incremental Floorplanning

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ABSTRACT

The current integrated circuit design trend is towards high performance, low power, high density as well as heterogeneous integration. Traditional two-dimensional integrated circuit (2D IC) design has been unable to meet nowadays need of IC product. Hence, three-dimensional integrated circuit (3D IC) is emerging as an effective way for overcoming the barriers in 2D IC design. Though interconnection delay can been improved by 3D IC floorplanning, circuits are growing in complexity, so it is difficult to design an optimal layout solution. Therefore, to obtain a better result, it needs performing floorplanning repeatedly. However, the process will increase the time of physical design. To reduce the time of floorplanning, incremental floorplanning has been proposed to deal with local or incremental change of layout solution efficiently. To sum up, an incremental floorplanning system has beeb proposed for 3D ICs to guide 3D physical design towards an optimal layout solution in this thesis, and it has been developed based on mathematical programming. In the first of the procedure, the changed modules and whitespace around them are found in the original floorplan, and then the final layout is obtained without the change of topology among modules and without the increase of chip size. The whole procedure has been implemented by integer linear programming method and been solved by LINGO software. Experimental results show that it is effective for this incremental floorplanning system to change modules and improve interconnection delay problem.

Keywords : 3D IC、Incremental Floorplanning、Integer Linear programming

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