Simultaneously Considering Layout Area and TSV Wire Length on TSV Placement for 3D IC

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ABSTRACT

The semiconductor industry into the 3D IC technology and Through Silicon Vias (TSV) technology become increasingly important. On the same circuit design, 3D IC achieves high density, low power consumption and good timing slack. Chemical-Mechanical Polishing (CMP) technology is an important procedure in the fabrication of chip to enhance the overall smoothness need for increasing the yield. 3D IC technology will stack multiple chips using TSV as the components of the signal between the chip. But the TSV ’ s size is larger than the other functional cell, the metal density of the TSV region is extremely high. It ’ s a challenge to the traditional CMP planarization flow of 2D IC design. In this paper, we proposed a TSV placement flow which takes chips density and TSV ’ s wire-length into account. The proposed method will consider the TSV ’ s wire-length, and place TSV in the layout of lower density to solve the density difference in the layout. Experimental results show that to placed TSV by the factor of density differences method increase the wire-length by 2.11%-24%, but can reduce the amount of dummy fills by 4%-7.8% compared with the placed TSV method according to lowest density.

Keywords : 3D IC、TSV placement、CMP

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