同時考量佈局面積與TSV線長的3D IC 之TSV擺置方法設計

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摘 要

矽穿孔3D IC技術為將多個晶片堆疊，並使用矽穿孔(Through Silicon Vias；TSV)作為晶片間之訊號傳遞。矽穿孔3D IC 技術對於拉近晶片設計與製程技術的落差至為重要，由於使用3D堆疊，能使晶片面積縮小、提高訊號傳遞速度，並降低晶片功耗等效能，因此，矽穿孔3D IC技術日益重要。 然而，矽穿孔的孔徑較晶片晶元(Cell)與導線來的大，因此，會造成晶片佈局區域金屬密度大幅升高的現象，由於佈局的平坦度更加惡化，使得CMP研磨的挑戰更高，傳統2D IC的密度分析與虛擬金屬填充方法也不適用。 本文提出同時考量佈局面積與矽穿孔線長的3D IC矽穿孔擺置方法之設計，在佈局密度較低與密度差異較大的區域，進行矽穿孔安插；並考量與矽穿孔連線的元件位置來安插矽穿孔，可將原本繞線密度低的區域縮小密度差異，以解決密度差異過大而影響佈局的平坦度。矽穿孔擺置方式會分為密度最低與密度差異大兩種策略，由實驗結果可見本文所提出的方法，在佈局平坦度上能獲得良好的成效，且虛擬金屬添加量能有效的降低，其中密度差異大的擺置策略比密度最低的擺置策略，虛擬金屬添加量減少了4%-7.8%。若以矽穿孔連線長度而言，密度差異大的擺置策略的結果在線長多了2.11%-24%。

關鍵詞 : 3D IC、矽穿孔擺置、CMP平坦化、3D晶片平坦化

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