

The Implementation of an Reed-Solomon Decoder with CPU Technology

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ABSTRACT

The implementation of Reed Solomon decoding is realized by VHDL programming, which includes operations of CPU and RAM. The firmware program operated in CPU is with MIPS instruction formats, and stored in a block of RAM. MIPS instructions with the length of 32 bits are employed in this firmware program, which contains syndrome computations, error location polynomial calculations, error location searches, and error corrections. In this work, we also design a codespim platform to modify some instructions and reduce the size of the firmware program. In such a way, the decoding speed is faster and implementation is realized with Modelsim.

Keywords : Reed-Solomon code

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