3D stacked IC layout considering TSV and metal density for CMP planarization / 賴永埼 撰 .- 彰化縣大村鄉

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ABSTRACT

In modern semiconductor industry, 3D IC technology and through silicon vias (TSV) technology become increasingly important. 3D IC achieves high density, low power consumption and good timing slack. chemical-mechanical polishing (CMP) technology is an important procedure in the fabrication of chip to enhance the overall smoothness need for increasing the yield. Because of the TSV ’s size is larger than the other functional cell, the metal density of the TSV region is extremely high. It ’s a challenge to the traditional CMP planarization flow of 2D IC design. In this thesis, we proposed a CMP planarization flow which takes TSVs into account. The proposed method builds a bounding box around each TSV, and calculates the amount of dummy fills with respect to the routing density outside the bounding box for CMP planarization. Experimental results show that the proposed method can reduce the amount of dummy fills by 12%-36% compared with the 2D IC dummy fills insertion.

Keywords : 3D IC、TSV、Chemical-Mechanical Polishing

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