基於推導線與重繞線的佈局密度優化方法 = Layout density optimization with wire pushing and rerouting for CMP planarization

陳冠中、林浩仁, 程仲勝

E-mail: 354784@mail.dyu.edu.tw

摘 要

化學機械研磨(Chemical-Mechanical Polishing；CMP)技術的形成是目前後端製程所必經的步驟，為了提高CMP程序後整體佈局的平坦?，需在晶片佈局中添加虛擬?屬(Dummy Fill)填充。在安插虛擬?屬至晶片佈局前，必須先對晶片佈局做密?分析，並計算需要安插多少虛擬?屬數量置晶片佈局的。本文提出推導線與重繞線方法，?進?降低初始晶片佈局密度不均勻的情況，固定分割在計算安插多少虛擬?屬數量至方格(Tile)中，會有為了提昇平坦度目標，而造成虛擬?屬數量上使用過多的情況發生，而本文提出推導線與重繞線方法，目的在可以降低虛擬?屬的使用成本。以ISCAS89 測試電?的實驗?據顯示，本文提出的推導線與重繞線方法，可以節省虛擬?屬使用數量達12%到22%。

關鍵詞 : 平坦化、CMP 平坦化技術、虛擬?屬

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