

Noise-Aware Optimization Technique for MTCMOS Circuits

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ABSTRACT

As integrated circuits design technology scales into deep submicrometer regime, subthreshold leakage current and crosstalk noise are two more than more important questions in IC design. Due to Multiple Threshold Voltages CMOS(MTCMOS) technology is an effective way to reduce subthreshold leakage current without increase design complexity. This paper provide a way that focus on crosstalk to use MTCMOS technology on the areas that have serious crosstalk with High-V_{th} device. As High-V_{th} device have more good resistance than Low-V_{th} device when crosstalk occur, so we use High-V_{th} device to replace Low-V_{th} device that on the serious crosstalk area. But High-V_{th} device have high delay time of signal so we must consider timing constrain when use MTCMOS technology. We provide a way that replace High-V_{th} device with aggressor nets and victim nets alternately.

Keywords : MTCMOS、HVT、RVT

Table of Contents

封面內頁 簽名頁 中文摘要.....	iii	ABSTRACT.....	iv	致		
謝.....	v	目錄.....	vi	圖目錄.....	viii	表目
錄.....	ix	第一章 緒論.....	1	1.1 前言.....	1	1.2 耦合雜
訊.....	2	1.3 功率消耗.....	4	1.4 研究動機.....	6	1.5 論文架
構.....	8	第二章 文獻回顧.....	9	2.1 文獻回顧與探討.....	9	2.2 常見改
善雜訊方法.....	9	第三章 考量雜訊之MTCMOS電路優化演算法.....	12	3.1 MTCMOS技術簡		
介.....	12	3.2 耦合雜訊導向之V _{th} 值選擇策略.....	13	3.3 Aggressor Net 置換策略.....	14	
3.4 Victim Net 置換策略.....	16	3.5 程式流程.....	18	第四章 實驗結		
果.....	22	4.1 實驗環境與測試電路.....	22	4.2 實驗過程與結果分析.....	24	4.3
改善前後侵害線段分析與探討.....	26	4.4 改善前後受侵害線段分析與探討.....	28	4.5 改善前後整體耦合雜		
訊分析與探討.....	31	第五章 結論與未來展望.....	33	5.1 結論.....	33	5.2 未來展
望.....	33	參考文獻.....	35			

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