考量雜訊之MTCMOS電路優化演算法

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摘 要

由於積體電路製程越來越先進使得目前奈米世代積體電路的耦合雜訊與漏電流的問題越來越嚴重，又因Multiple Threshold Volt?ages CMOS(MTCMOS)製程技術可以再不增加電路設計的複雜度下有效降低漏電流是近年來相當受到重視的方法。本篇論文提出加入耦合雜訊的觀點使用MTCMOS之技術在佈局中耦合雜訊嚴重之區域使用High-Vth來替代原本Low-Vth元件來達到降低耦合雜訊的干擾，由於High-Vth元件的雜訊免疫力較Low-Vth元件高，可以有效降低Low-Vth元件在因雜訊干擾導致元件功能運算錯誤的情形但由於High-Vth元件擁有較高延遲的缺點所以必須同時考量整體訊號時序是否造成錯誤的問題，本論文將耦合雜訊干擾線段分為Aggressor Nets與Victim Nets 並以交互使用MTCMOS之技術不同於以往單一考量某一種線段的置換方式來實做。

關鍵詞 : 耦合雜訊干擾、雜訊

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