A circuit partitioning algorithm for 3D IC designs

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ABSTRACT

The current integrated circuit design trend is towards high performance, low power, high density as well as heterogeneous integration. Traditional two-dimensional integrated circuit (2D IC) design has been unable to meet nowadays need of IC product. Hence, three-dimensional integrated circuit (3D IC) is emerging as an effective way for overcoming the barriers in 2D IC design. In Taiwan, 3D IC technology has also become a very important and hot issue for IC design companies. 3D IC needs 3D chip architecture to implement the whole design. That is, the whole circuit must be divided into several subsystems, and each one should be implemented on single layer of die. 3D IC chip can thus be formed by stacking these layers of dice vertically. Besides considering chip manufacture cost same as 2D, 3D chip cost also consists of die stacking cost, stacking yield, TSV(through-silicon-via) cost and TSV yield to reflect heat dissipation and TSV insertion problems. To meet the goal of 3D IC design, in this thesis, based on 3D cost evaluation function, a 3D IC circuit partitioning procedure considering TSV minimization is proposed. The experimental results show that the proposed algorithm demonstrates the improvements on the minimization of TSV.

Keywords : 3D IC、circuit partitioning、TSV

Table of Contents

封面內頁 簽名頁 授權書iii 中文摘要iv ABSTRACTv 誌謝vi 目錄vii 圖目錄ix 表目錄xi 第一章 緒論1 1.1 研究動機與目的1 1.2 研究方法2 1.3 論文架構3 第二章 3D IC相關文獻探討4 2.1 3D晶片技術整合4 2.1.1 封裝堆疊4 2.1.2 晶片堆疊6 2.1.3 TSV堆疊7 2.2 TSV 3D IC堆疊技術8 2.3 3D IC分割演算法11 第三章 3D IC電路分割演算法12 3.1 問題描述12 3.2 3D IC分割演算法15 3.3 HMETIS分割演算法16 3.4 產生最佳初始堆疊20 3.5 減少TSV數量之策略28 3.5.1 策略一：層間互換28 3.5.2 策略二：模擬退火29 第四章 實驗結果32 4.1 產生最佳初始堆疊順序33 4.2 層間互換36 4.3 模擬退火38 4.4 面積限制與TSV數量變化41 4.5 堆疊層數與TSV數量變化45 4.6 不同演算法比較51 第五章 結論與未來展望55 參考文獻56

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