

# 一個適用於3D IC設計之電路分割演算法

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## 摘要

積體電路設計已進入高效能、低功率、高密度以及異質整合的時代，傳統2D IC設計漸漸地已無法滿足現今IC產品之需求，因此IC設計朝向三維方式發展已是目前克服設計困難度的最有效方式之一。以國內而言，3D IC設計技術已是各家IC設計公司及半導體製造廠商目前最熱門的議題及發展重點之一。3D IC設計是將所有電路整合在三維晶片上，亦即需將電路分割成幾個子電路系統，而每個子系統可實作在單一層裸晶上，每個裸晶在垂直方向堆疊整合成一個3D IC。3D晶片製作成本除需考量2D晶片製作成本外，因其堆疊整合會有較嚴重的散熱問題及需安插矽穿孔(through-silicon-vias, TSVs)以利連接各層訊號線，必須額外考量裸晶堆疊成本及其良率、TSV成本及其良率等問題。為了符合3D IC設計問題，本論文中我們在植基於一個考量上述各因素之分割成本函數下，提出一個能有效減少TSV數量之3D IC電路分割。實驗數據顯示我們提出的演算法確實可以有效地減少TSV使用的數量。

關鍵詞：3D IC、電路分割、TSV

## 目錄

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