Implementation of a turbo-code decoder with Pade approximation by using the dual-core MIPS-like processor

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ABSTRACT

Turbo coding offers excellent capabilities of error correction and thus has been getting popular in the wireless applications. Turbo codes demonstrate a means of closely approaching the Shannon capacity of communication channel. In this study, a Turbo-code decoder with Pade approximation using the dual-core RISC MIPS-like processor in association with the Verilog HDL and ASM is developed. A turbo-code codec with pade approximation is developed using Visual Basic language in this study. The encoded message from the codec designed by VB is imported the turbo-code decoder with pade approximation designed by C language for the verification. The C design of the turbo-code decoder is further compiled by GCC to generate the MIPS assembly. The machine code generated by PCSpim can be further embedded into shared memory of the dual-core MIPS-like processor designed by Verilog hardware description language and algorithmic state machine. The system simulation by using ModelSim and hardware verification by using FPGA are found to be correct. Finally, the MIPS-like processor is implemented with VLSI layout under TSMC 0.35 μ m process technology and to be able to produces the chipset in CIC. The main contribution of this study is using dual-core MIPS-like processor and integrating various EDA tools to achieve VLSI layout that the C design can be rapid prototyped in FPGA chip for verification. In this work, The bit-error-rate (BER) performance of proposed Pade-approx-log-MAP algorithm is superior to those of previous log-MAP algorithms such as max-log-MAP, constant-log-MAP, and linear-log-MAP.

Keywords : FPGA、MIPS、Pade approximation、turbo code、Dual-core

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