ABSTRACT

Designing modern computers' micro-architecture relies on dynamic instruction traces for design optimization. However, dynamic instruction traces often generate massive data that make the traces difficult to analyze and process. This thesis proposes a novel dynamic instruction traces profiling framework and a profiling algorithm named Melting in mining the most frequent and longest instruction sequence. The profiling framework is exemplified by designing memory hierarchy for JPEG image compression algorithm. The proposed profiling framework combines both the merits of traditional functional profiling and modern instruction traces schemes. The framework is divided into two steps. The target program is first profiled using a function level profiler where the most frequent function is determined. The derived function is simulated using the SimpleScalar/ARM 4.0 simulator where dynamic instruction traces is generated. As a result, the amount of traces data is greatly reduced. Finally, having the traces obtained, the Melting Algorithm is applied to mine the most frequent and longest consecutive instruction sequence. The mined sequence is applied to optimize memory hierarchy. The sequence can also be applied in instruction compression and other micro-architecture design issues.

Keywords: Data mining; Cache design; SimpleScalar; JPEG; ARM

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