

Analysis of PCB Trace Layout Effect on the EMI Crosstalk

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ABSTRACT

The rise time of signals in PCB (Printed Circuit Board) circuit become shorter, and high speed transmission and high density packing have become the trend of PCB development. Therefore the noise affects transmission loss which increases to error action on a PCB circuit under high frequency operation. One of the most common noise sources in PCB system is the crosstalk noise. The source occurs on parasitic mutual capacitance in conjunction with mutual inductance between adjacent conductors. The problem become more as we increase the density of PCB trace layout. One advantage of a well-designed signal system is that it can provide protection against unwanted interference and emissions, without any additional per-unit cost to the product. The only cost is the study time to design a PCB layout frame. Therefore we require considerable engineering time to eliminate the factor and reduce testing and debugging in the later development. In this thesis, the 3W and 20H are the regular PCB layout rule to confer the with optimum layout frame. In the finite PCB layout area, we add a grounded guard trace to reduce the emission coupling of the crosstalk. Several types of layout module for reducing the products cost and layout area of PCBs . The experiment uses the vector network analyzer to measure the crosstalk and IE3D numerical simulations to compare with the accuracy of the measured results. It can offer the best choice for the PCB layout style, to carry out the related testing procedure for reducing the unwanted EMI effects.

Keywords : 3W、20H、PCB Layout、Crosstalk、Grounded Guard Trace

Table of Contents

封面內頁 簽名頁 授權書	iii	中文摘要	
. iv 英文摘要		v 誌謝	
. vi 目錄		vii 圖目錄	
. ix 表目錄		xii 第	
一章 序論	1	1.1 前言	
. 1.1.2 研究動機	2	1.3 論文提要	
. 2 第二章 基本理論	4	2.1 互容互感原理	
. 4.2.2 傳輸線方程式	11	2.3 20H-Rule	
. 18 2.4 3W-Rule	20	第三章 實驗環境設定	
. 23 3.1 實驗設計概念	23	3.2 測試	
基板之型態	23	3.3 實驗設定與範圍	
26 3.4 量測環境的架設	29	3.5 IE3D數值模擬	
. 33 第四章 量測與模擬結果分析	36	4.1 3-W與20-H Rule量測與模擬	
. 36 4.2 兩傳輸導線間增加一接地防護導線對S41輻射耦合量之影響			
. 38 4.3 接地防護導線的寬度變化對S41輻射耦合量之影響			
. 38 4.4 縮小接地導體面的面積(10H至5H)並改變接地防護導線的位置對S41輻射耦合量之影響			
. 39 第五章 結論	61	參考文獻	
. 63			

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