ABSTRACT

With the advanced processing, the difference region between supply voltage and threshold voltage is scaled gradually. The scaled noise margin causes the leakage current to be one of the critical issues in the very deep submicron designs, and will seriously cause unnecessary power consumption. Domino keeper is always using to keep the noise margin in high fan-in domino gate. However, both the increasing power consumption and slower performance are significant problems due to the causing DC contention. In this paper, we present a new high-speed domino technique, called Conditional Isolator Domino (CI-Domino), for wide fan-in domino logic. The CI-Domino logic not only improves the noise margin without sacrifices performance, moreover, subthreshold current can be significantly reduced in CI-Domino operations. By the simulation results on 0.18μm processing, CI-Domino significantly achieves the 48.14% noise margin improvement respective to conventional domino in the comparison of 32 fan-in OR gate, and further, CI-Domino reduces active power by 49.14%, standby power by 35.99%, and delay time by 60.27%.

Keywords: Noise Margin, Leakage Current, Domino Logic Circuit, DC Contention, Subthreshold Current, Dynamic Power, Static Power, Delay time.


