Hazard Filtering Technique for Low-Power Circuit Design

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ABSTRACT

The close relationship between power consumption and heat dissipation makes low-power design techniques important knowledge for every CMOS designer. Of course, low-power circuit design is especially important in battery-operated systems like cellular telephones, personal digital assistants (PDA), wristwatches, hearing aids, pocket calculators, pagers and prospectively the handheld multi-media terminal. Battery-powered systems require consuming low power, so it is important to avoiding unnecessary activity to save the energy. This is the reason why we introduce the hazard elimination technique to achieve the low power consumption. Note that, eliminating hazard not only decreases the power consumption, but also reduces the function errors of circuits. The organization of this thesis is as follows. Chapter 1 introduces the low power developing condition and feature. Chapter 2 introduces the cause of the power consumption, and proceeds with the methods of reducing power consumption. Chapter 3 introduces three kinds of hazard (i.e., static-1 hazard, static-0 hazard, and dynamic hazard) and hazard filtering techniques. In chapter 4, we use a full adder as an example to illustrate our method, thinking about architecture, circuit design, flooring layout, and routing for the purpose of obtaining low-power and high-speed circuits. We simulate the circuits using Hspice simulator. The chip is fabricated in TSMC 0.35um technology. Finally, we make a conclusion in Chapter 5.

Keywords: low power circuit design, hazard

REFERENCES


