Abstract

Recently, Poly-silicon Thin Film Transistors have received extensive attention for their potential application in printhead, imager, large-size active-matrix liquid crystal display (AMLCD). Typically, TFT operates with a floating substrate and the operation bias is about 12V. Moreover, the characteristics of TFT are severely affected by material properties of poly-silicon. As a result, the characteristics of a TFT cannot be accurately modeled by the common bulk MOSFET model in SPICE. Quite a few circuit models for low temperature poly-silicon TFT have been reported, but very few of them took the temperature effect into account. So far, none have been implemented into commercially available circuit simulator with temperature dependent features.

The work attempts to develop a physically-based analytical current-voltage model and an intrinsic capacitance-voltage model of poly-Si TFT for circuit simulation. First, we have developed a set of programs including I-V and C-V models and parameter extraction methods. The model parameters are extracted from the experimental data and then substituted back into the developed models. The accuracy of these models were successfully implemented in MEDICI, TSUPREM4, AIM-SPICE. The experimental data used here are measured from an AMLCD wafer with a substrate and undergate structure. The device models are finally implemented in the AIM-SPICE circuit simulator to predict and analyze the circuit performance of poly-si TFT. A model, described for applications from the subthreshold to saturation regions that is continuous and differentiable, is suited for MEDICI, TSUPREM4, AIM-SPICE circuit simulator, in this thesis. Channel Length Modulation (CLM), Velocity Saturation (VS), Kink Effect (KE), Temperature Dependence Effect (TDE), Drain Induced Grain Boundary Potential Barrier Lowering (DIBL), Gate Induced Grain Boundary Potential Barrier Lowering (GIBL), Hot Carriers Effect (HCE) are discussed and modeled.

Keywords: Poly-silicon Thin Film Transistors; Channel Length Modulation (CLM); Kink Effect (KE); Drain Induced Grain Boundary Potential Barrier Lowering (DIBL)


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